

# Compal Confidential

## Intel MB Schematic Document

2019 OMEN 17.3" Santorini  
FPC72 LA-H492PR01

Date : 2018/09/28

Version: v0.1

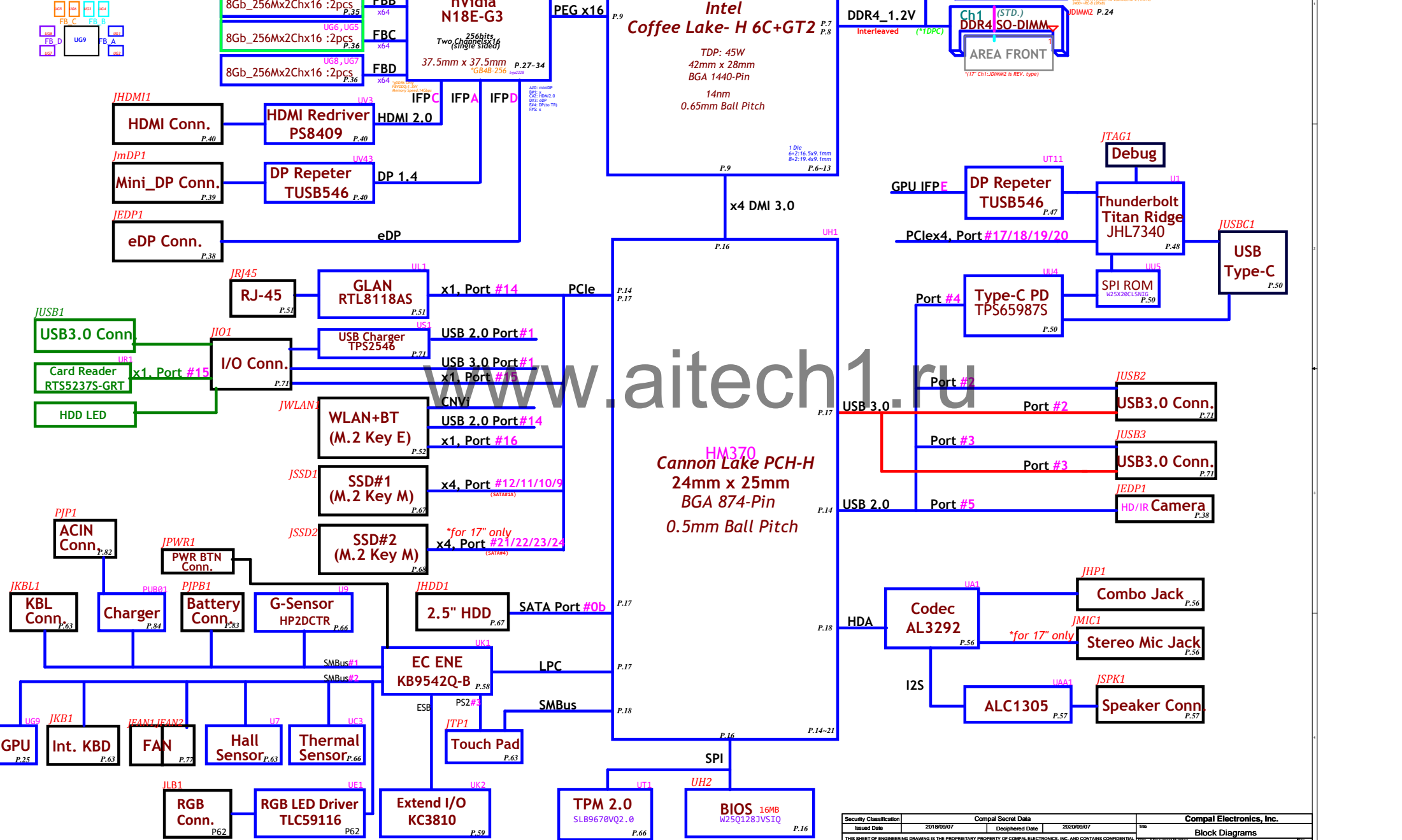
15.6": FPC54 LA-H481PR(N17)  
LA-H482P(N18)  
17" : FPC72 LA-H491P(N17)  
FPC72 LA-H492P(N18)

(Modified&Ref from: 01."DPF50\_LA-F842PR1A\_201800411(PPAV)")  
02.GPU:"DPF50\_LA-F863PR01\_180723(PPAV)"  
03.GPU reference:"EH78F\_LA-G161PR01\_0810")

15" to 17" different:  
01. Add SSD#2  
02. Combo HP Jack to separated MIC jack  
03. J1MM2 to STD. revision.  
04. Screw Location  
05. BATT from SMT to DIP  
06. ACIN CONN  
07. GPU Core from 6phase to 4phase

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N18E-G3: TGP:150 W / TDP:120 W / Memory TDP:17 W  
N18E-G3 MAX-Q: TGP:150 W / TDP:120 W / Memory TDP:17 W  
N18E-G3 MAX-Q: TGP:150 W / TDP:120 W / Memory TDP:17 W  
N18E-G3 MAX-Q: TGP:150 W / TDP:120 W / Memory TDP:17 W  
N18E-G3 MAX-Q: TGP:150 W / TDP:120 W / Memory TDP:17 W  
N18E-G3 MAX-Q: TGP:150 W / TDP:120 W / Memory TDP:17 W



Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID /PCB Revision	Rb	V <sub>AD_BTD_min</sub>	V <sub>AD_BTD_TYP</sub>	V <sub>AD_BTD_Max</sub>	EC AD3
0 --> 0.1	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
1 --> 0.2	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
2 --> 0.3	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
3 --> 0.4	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
4 --> 0.5					
5 --> 0.6					
6 --> 0.7					
7 --> 0.8					
8 --> 0.9					
9 --> 1.0					
10 --> 1.1					
11 --> 1.2					
12 --> 1.3					
13 --> 1.4					
14 --> 1.5					
15 --> 1.6					
16 --> 1.7					
17 --> 1.8					
18 --> 1.9					
19 --> 2.0					

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
CFL-H SKU	CFL_H@	
DGPU SKU	DIS@	
VRAM STRAP/3G	3G@	
VRAM STRAP/6G	6G@	
UMA	UMA@	
DIS	DIS@	
eSPI I/F	ESPI@	LPC@
TPM 9665	9665@	@9665@
TPM 9670	9670@	@9670@
CNVI	CNVI@	@CNVI@
EMI Components	EMI@	@EMI@
	VGAEMI@	
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@
XDP	XDP@	
ME Connector	CONN@	
STANDOFF	STD@	
For Signal Test	MP@	
VGA POWER SKU	VGA@	

HSIO Port Table(PCH)

HSIO Port	Capable	USB3.0	PCIE	SATA	Device	PCIE CLK&CLKREQ	NOTE
0	USB3.1_1 Gen1/Gen2	1			USB3.1 Port 1		
1	USB3.1_2 Gen1/Gen2	2			USB3.1 Port 2		
2	USB3.1_3 Gen1/Gen2	3			USB3.1 Port 3		
3	USB3.1_4 Gen1/Gen2	4			USB Type-C Port		TBT
4	USB3.1_5 Gen1	5					
5	USB3.1_6 Gen1	6					
6	USB3.1_7 Gen1	7					
7	USB3.1_8 Gen1	8					
8	HM370 disable						
9	HM370 disable						
10	/ GbE						
11	HM370 disable						
12	HM370 disable						
13	HM370 disable						
14	PCIE_9 / GbE		9				
15	PCIE_10		10				
16	PCIE_11 / SATA_0A		11	0	SSD-1	CLK2 & CLKREQ#2	
17	PCIE_12 / GbE / SATA_1A		12	1			
18	PCIE_13 / GbE / SATA_0B		13	0	HDD		
19	PCIE_14 / SATA_1B		14	1	Ethernet	CLK5 & CLKREQ#5	
20	PCIE_15		15		Card Reader	CLK3 & CLKREQ#3	
21	PCIE_16		16		WLAN	CLK1 & CLKREQ#1	
22	PCIE_17 / SATA_4		17	4			
23	PCIE_18 / SATA_5		18	5	Thunderbolt	CLK0 & CLKREQ#0	
24	PCIE_19		19				
25	PCIE_20		20				
26	PCIE_21		21				
27	PCIE_22		22				
28	PCIE_23		23				
29	PCIE_24		24		SSD-2 or Optane	CLK6 & CLKREQ#6	

Load BOM Option Table

BOM Number	Load BOM Option
431AAN32L01	3G@/XDP@/N17E_G1@/MP@/LPC@/DIS@/CNVI@/QNCT@/PCH@/DAX@/EMI@/ESD@/S3G@/H3G@
431AAN32L02	3G@/XDP@/N17E_G1@/MP@/LPC@/DIS@/CNVI@/QNVH@/PCH@/DAX@/EMI@/ESD@/S3G@/H3G@

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & CLKREQ#4	
DDI1	---		
DDI2	---		
DDI3	---		
eDP	---		PCH_EDP_HPD_R

Power State

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

USB2.0 Port Table

USB2	Function
1	USB3.1 Port 1
2	USB3.1 Port 2
3	USB3.1 Port 3
4	USB3.1 Type-C Port
5	
6	Camera/IR Camera
7	
8	
9	
10	
11	
12	
13	
14	WLAN+BT Module

GPU IFPx Table

Port	Function
A	mDP
B	--
C	HDMI 2.0
D	eDP
E	DP source to TBT
F	--

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM2	0X52	0XA4	0XA5
		TOUCH PAD			
PCH_SML0CLK PCH_SML0DATA	+3V_PCH_PRIM	NA			
PCH_SML1CLK PCH_SML1DATA	+3V_PCH_PRIM	EC	TBC	TBC	TBC
		GPU	0x4F	0X9E	0X9F

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBUS Port1	+3V_SMBUS	BAT	0x16	TBC	TBC
		CHGR	0x09	0x12	0x13
		G-Sensor	0x29	0x52	0x53
SMBUS Port2	+3VL	PCH	TBC		
		GPU	0x4F	0X9E	0X9F
		THERMAL	0x48	0X90	0x91
		PD (Default)	0x38	0X70	0x71
		Type-C MUX	0x10	0X20	0x21
			0x11	0X22	0x23

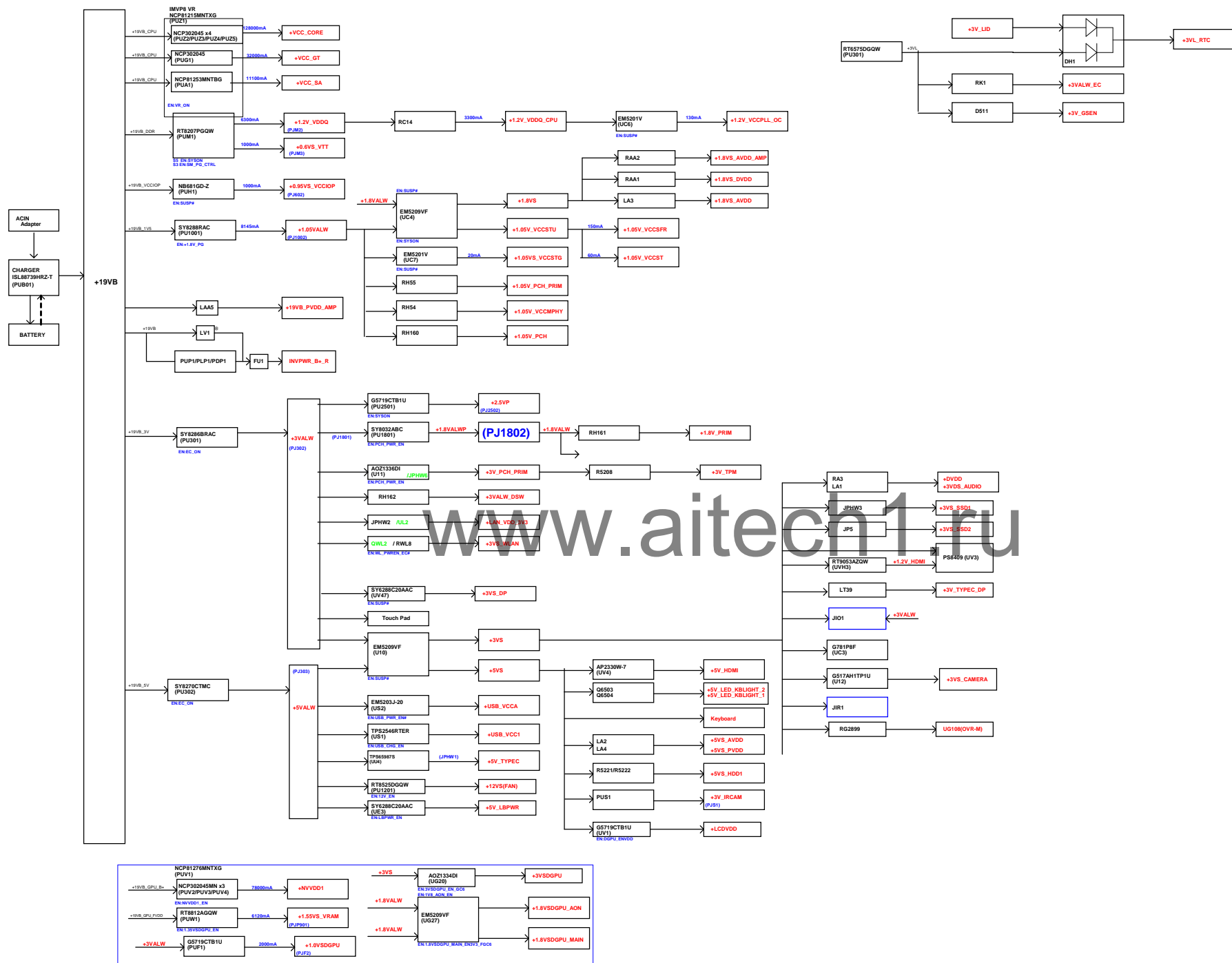
I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C_0_SCL I2C_0_SDA	+3V_PCH_PRIM				
I2C_1_SCL I2C_1_SDA	+3VS				

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.05VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	OFF	OFF	OFF
+1.05V_VCCMPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	+1.5VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF



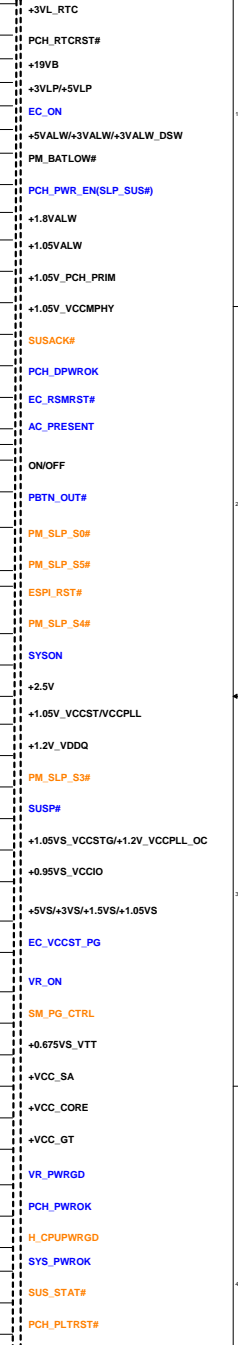
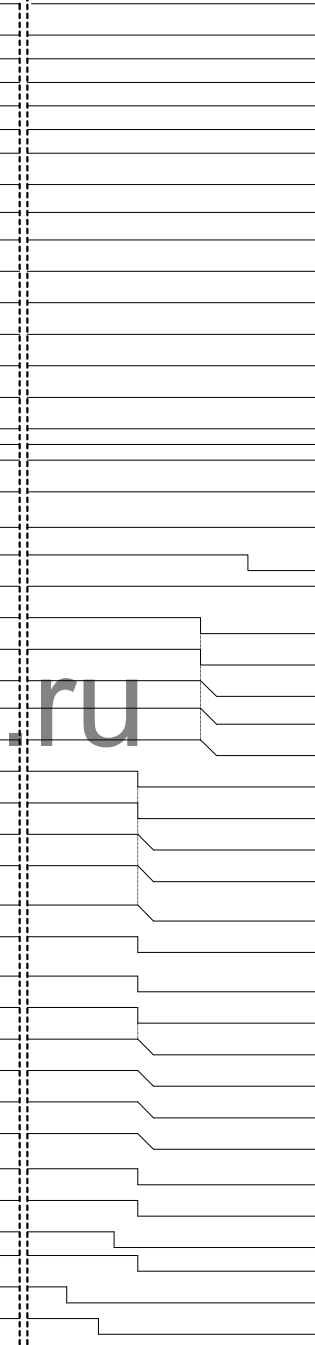
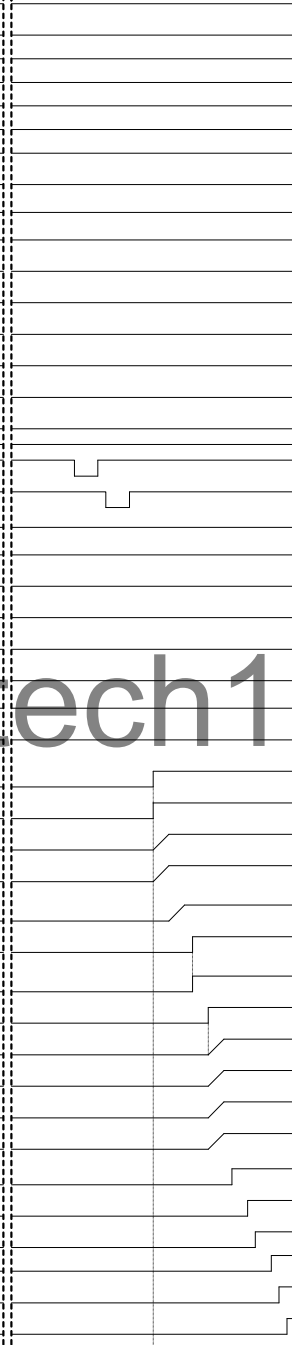
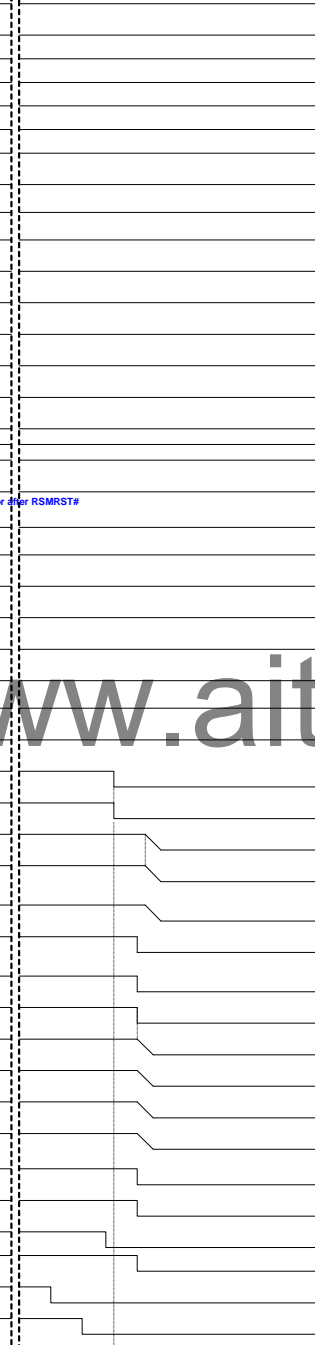
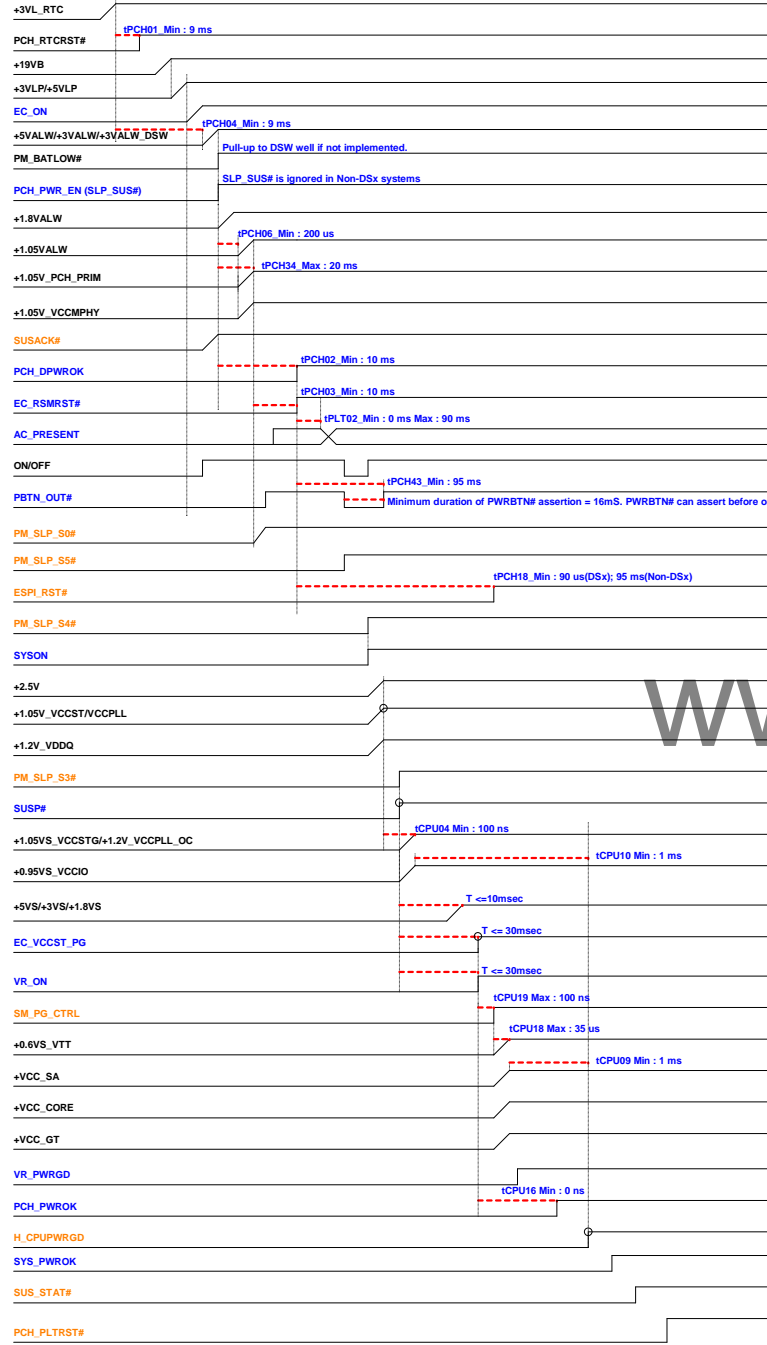


G3->S0

S0->S3

S3 ->S0

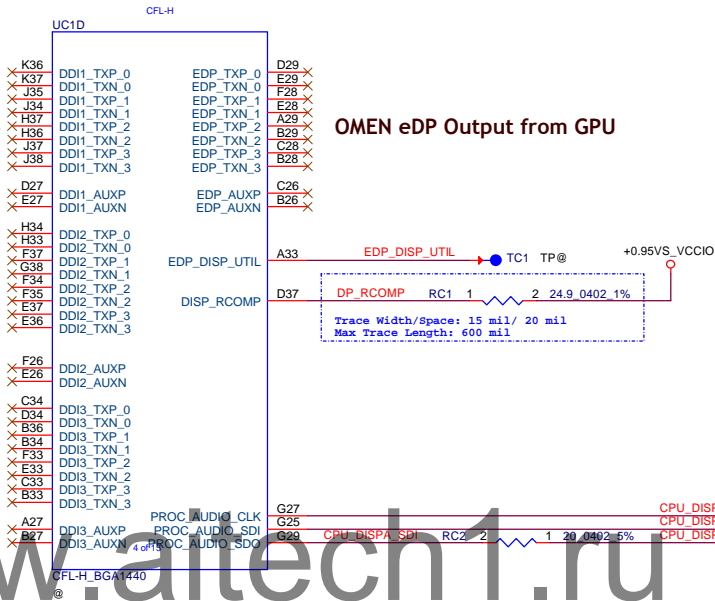
S0->S5



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OMEN: TR DDI input from GPU for DP v1.4

OMEN eDP Output from GPU

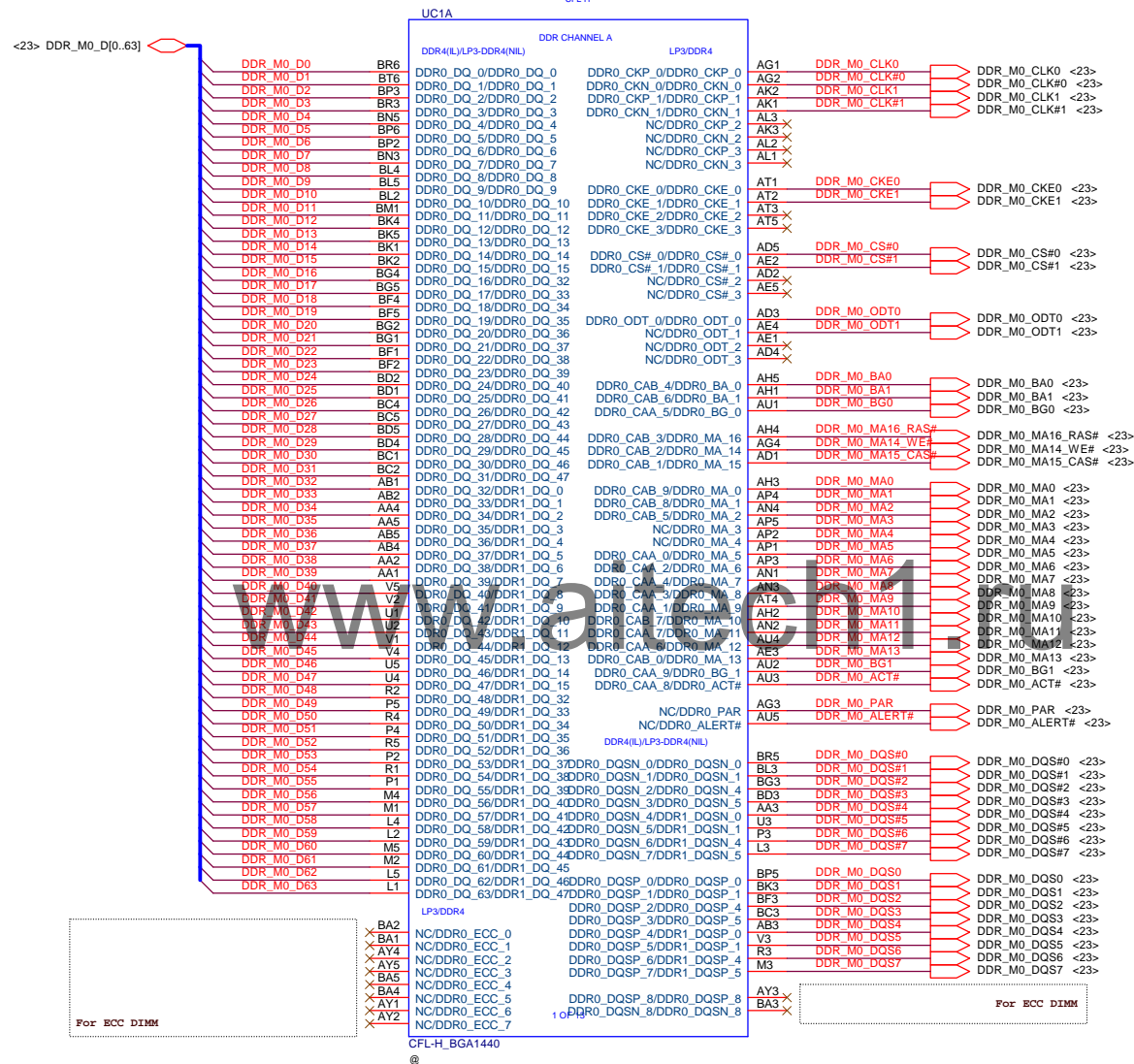


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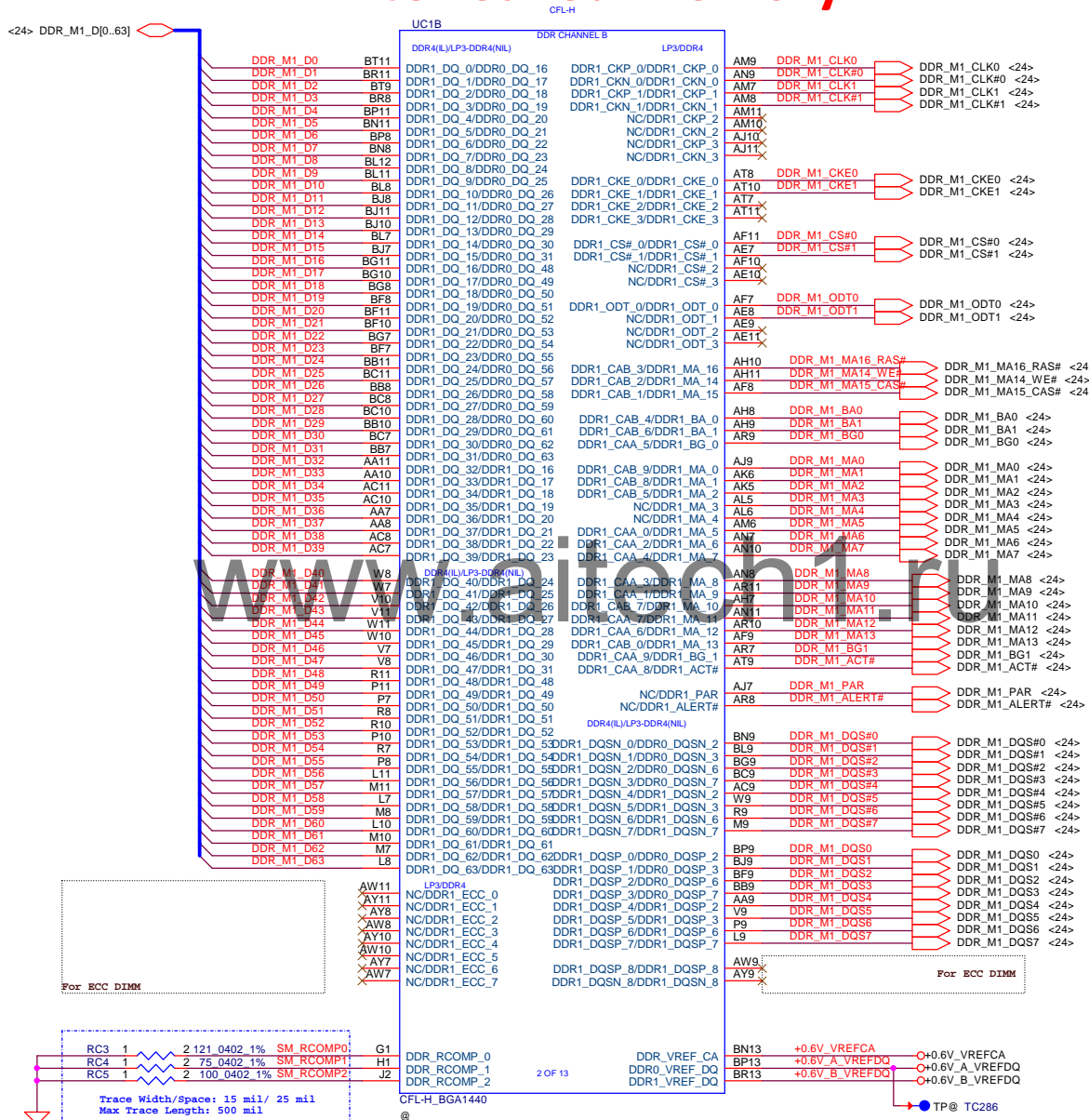
# CHANNEL-A

## Interleaved Memory



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# Interleaved Memory



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				New v0.1	

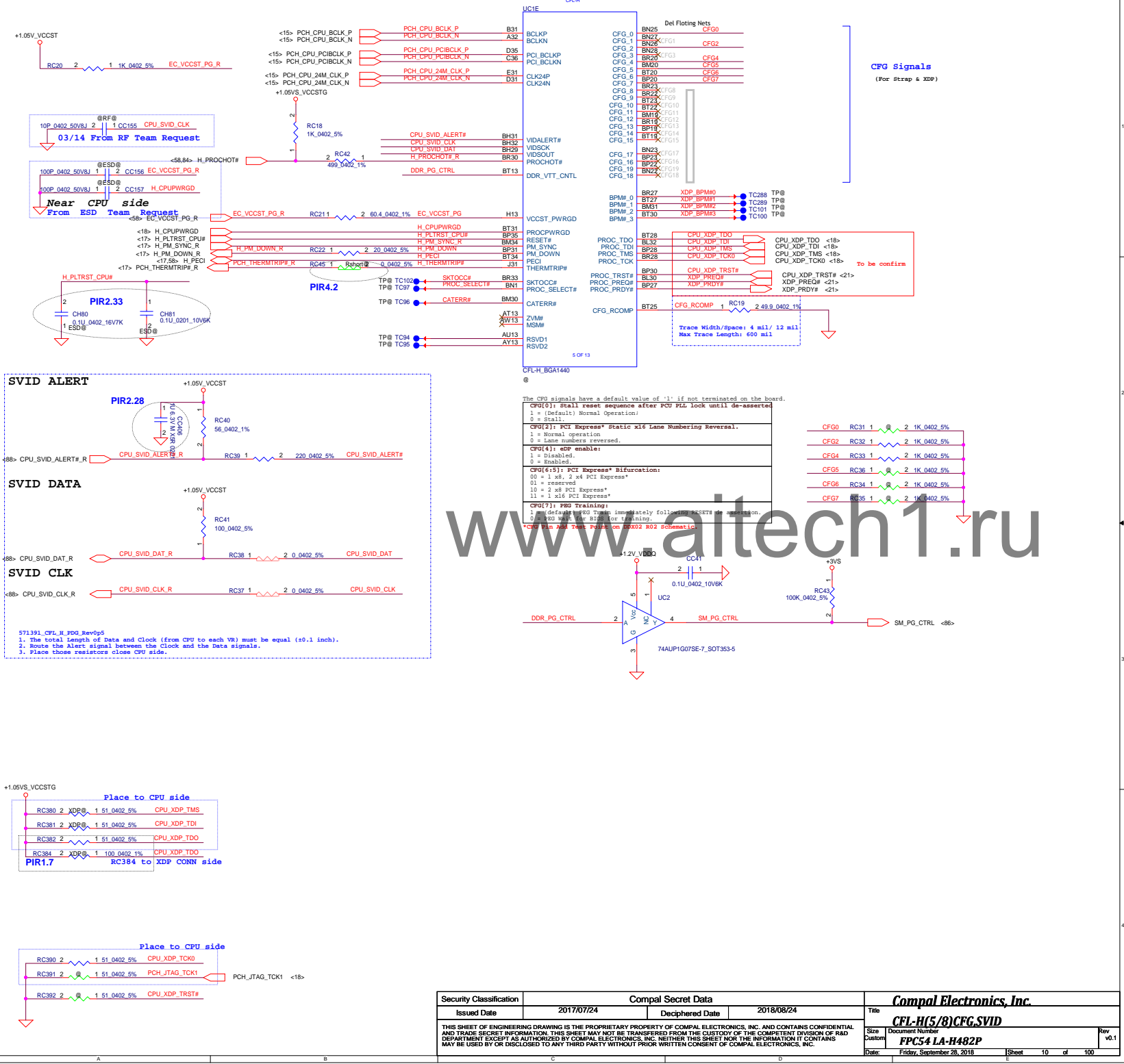
To DGPU  
PEG Lane Reversed

To DGPU  
PEG Lane Reversed

from PCH DMI[0:3]: RX

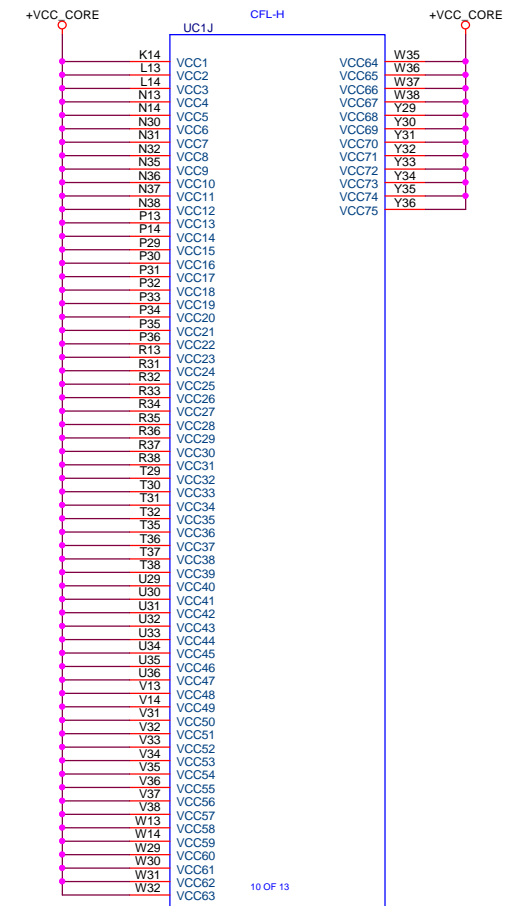
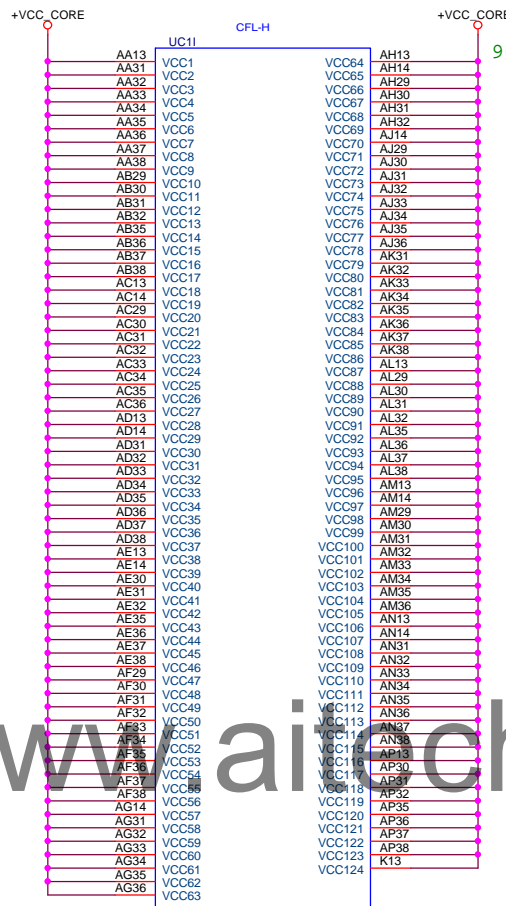
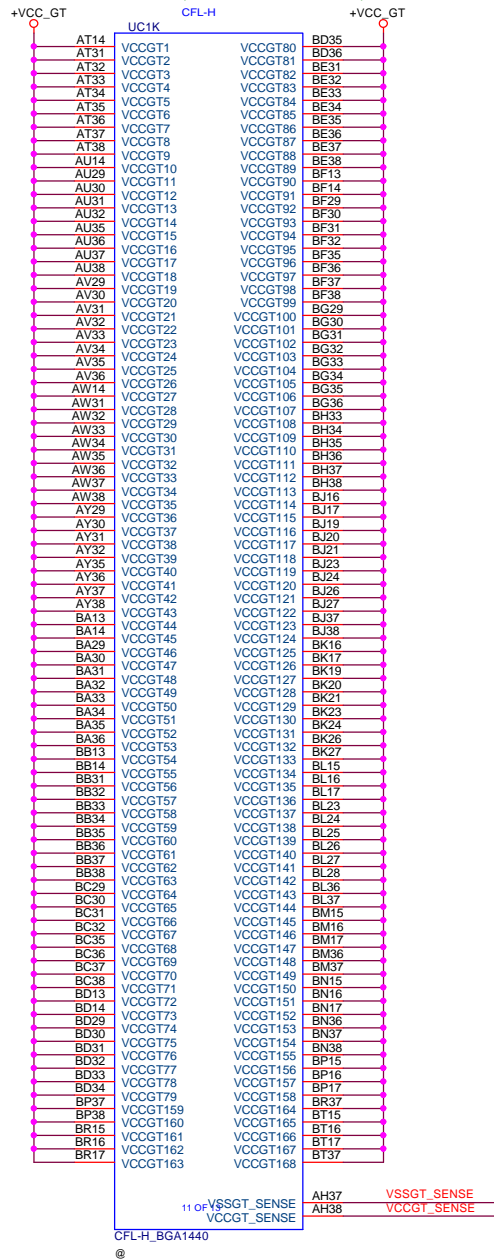
to PCH DMI[0:3]: TX

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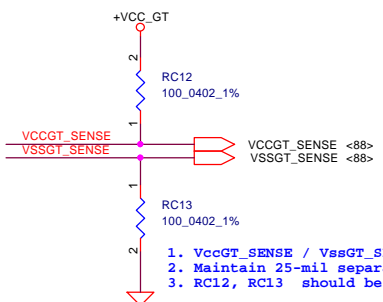




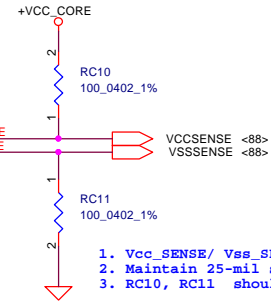
GT  
55000mA (Hexa Core GT2)



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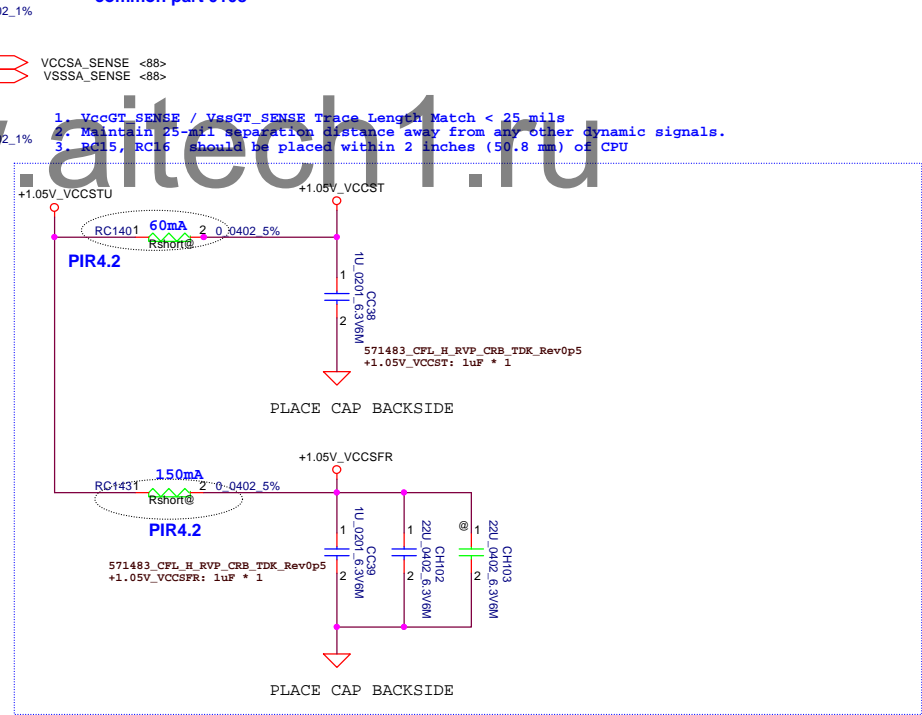
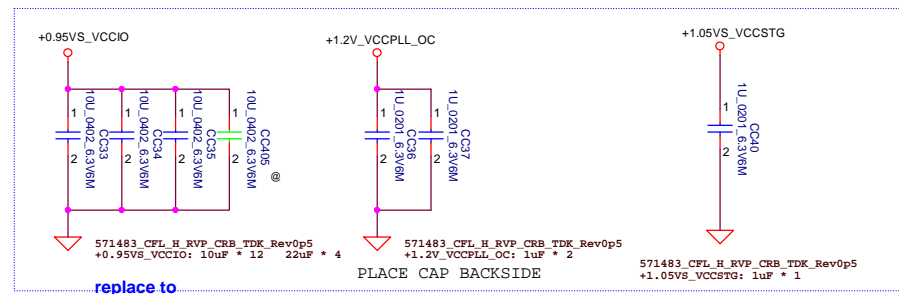
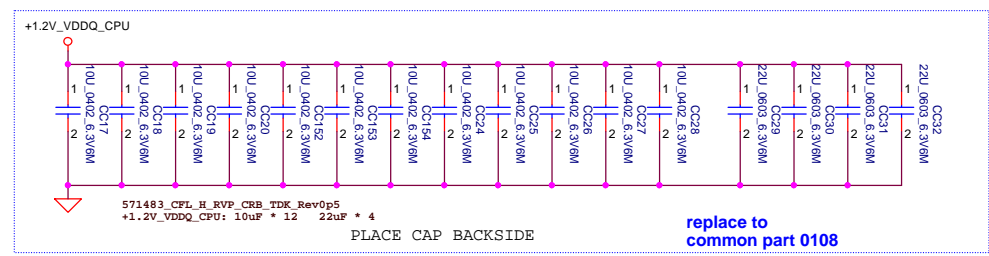
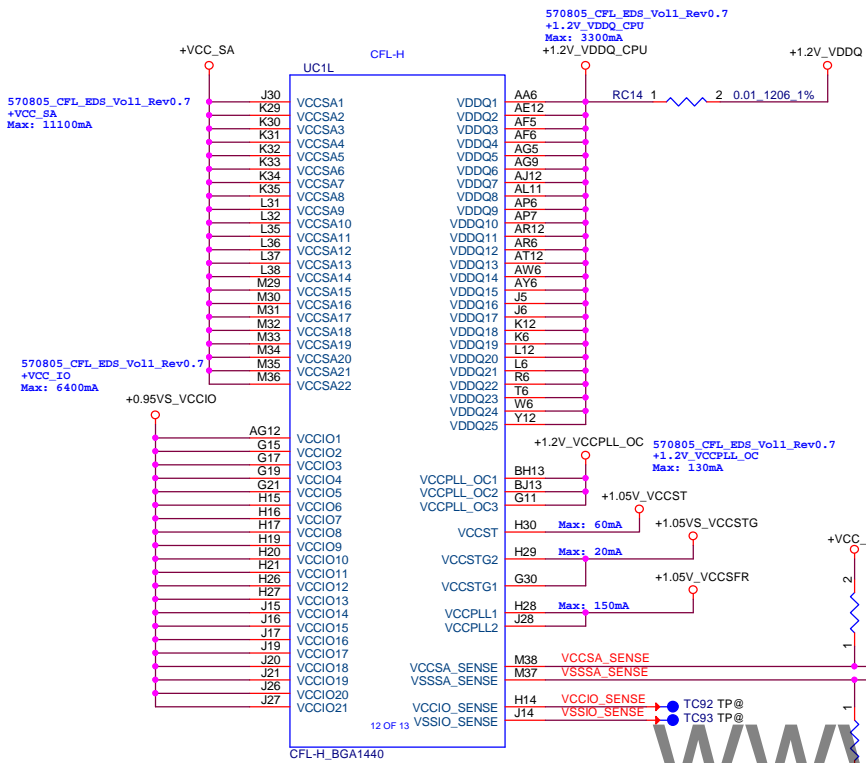


1. VccGT\_SENSE / VssGT\_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU



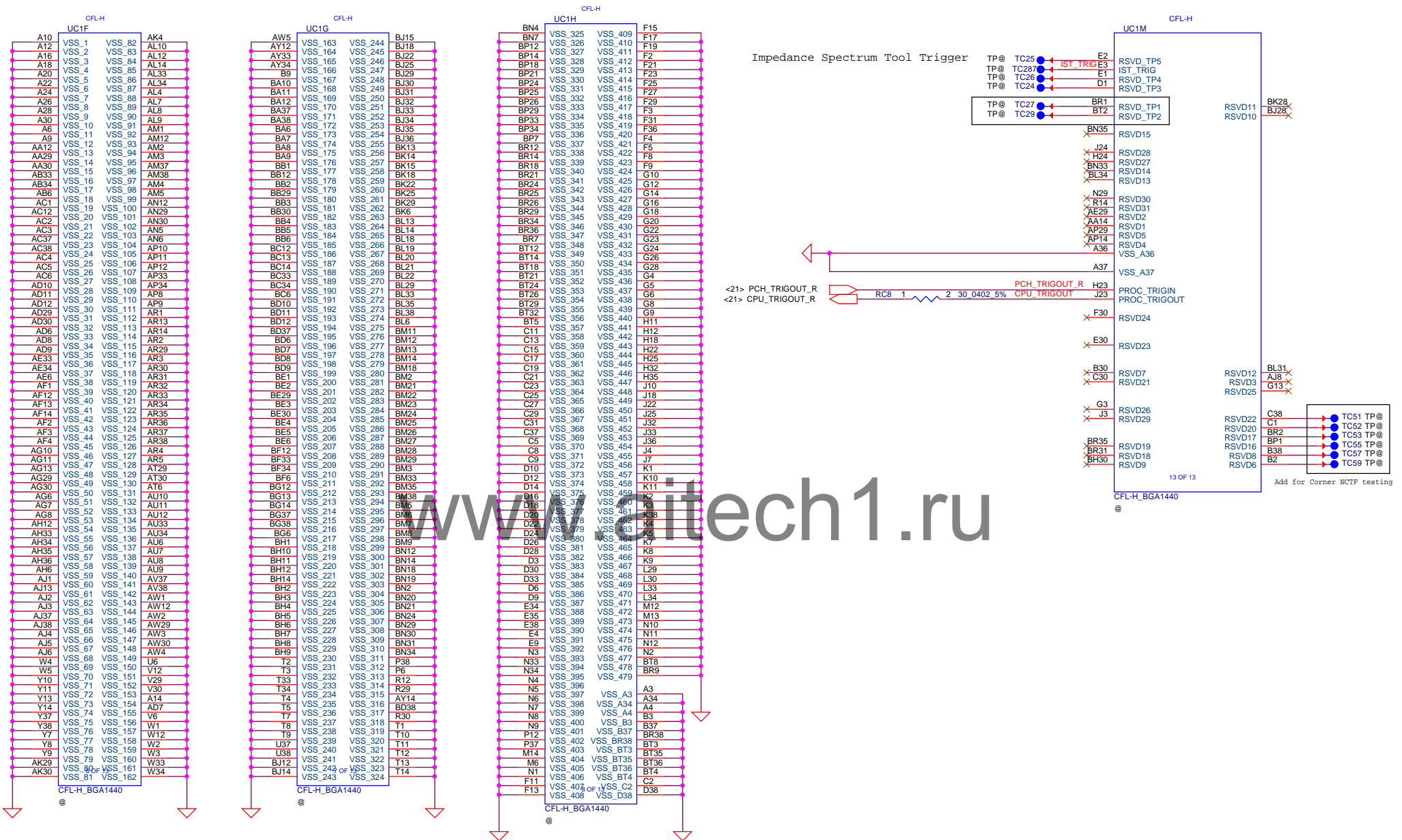
1. Vcc\_SENSE/ Vss\_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC10, RC11 should be placed within 2 inches (50.8 mm) of CPU

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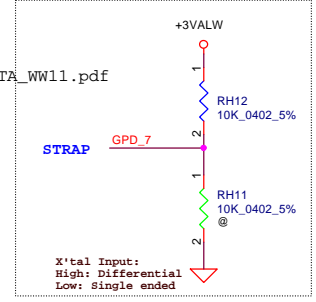
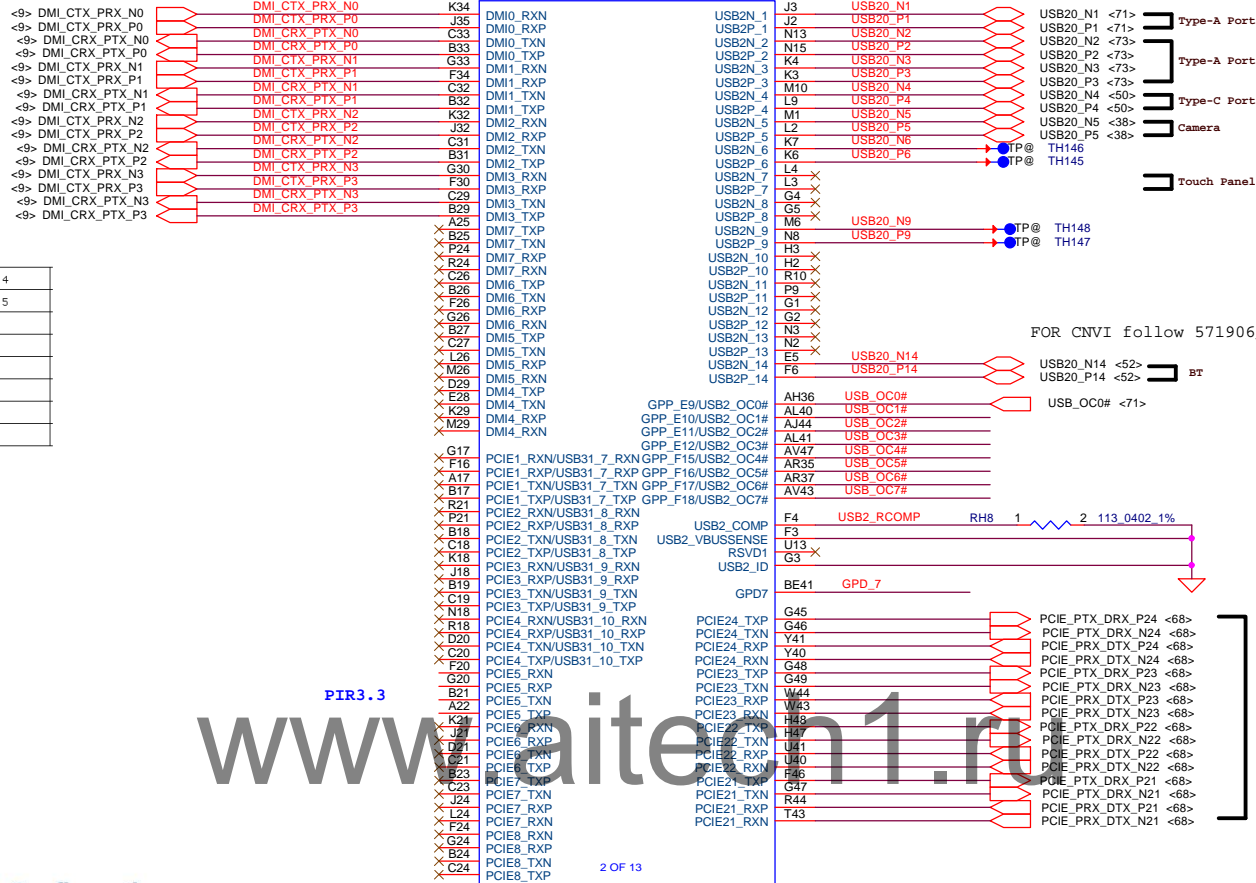




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from/to CPU DMI[0:3]:RX/TX

Flex I/O Lane	HM370		
0	USB3.1 Gen1/Gen2	22	PCIe*, SATA 4
1	USB3.1 Gen1/Gen2	23	PCIe*, SATA 5
2	USB3.1 Gen1/Gen2	24	PCIe*
3	USB3.1 Gen1/Gen2	25	PCIe*
4	USB3.1 Gen1	26	PCIe*
5	USB3.1 Gen1	27	PCIe*
6	USB3.1 Gen1	28	PCIe*
7	USB3.1 Gen1	29	PCIe*
8	N/A		
9	N/A		
10	GBE		PCIe Port 5
11	N/A		
12	N/A		
13	N/A		
14	PCIe*, GbE		
15	PCIe*		
16	PCIe*, SATA 0A		
17	PCIe*, GbE, SATA 1A		
18	PCIe*, GbE, SATA 0B		
19	PCIe*, SATA 1B		
20	PCIe*		
21	PCIe*		



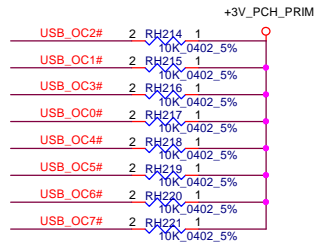
SSD #2[0:3]

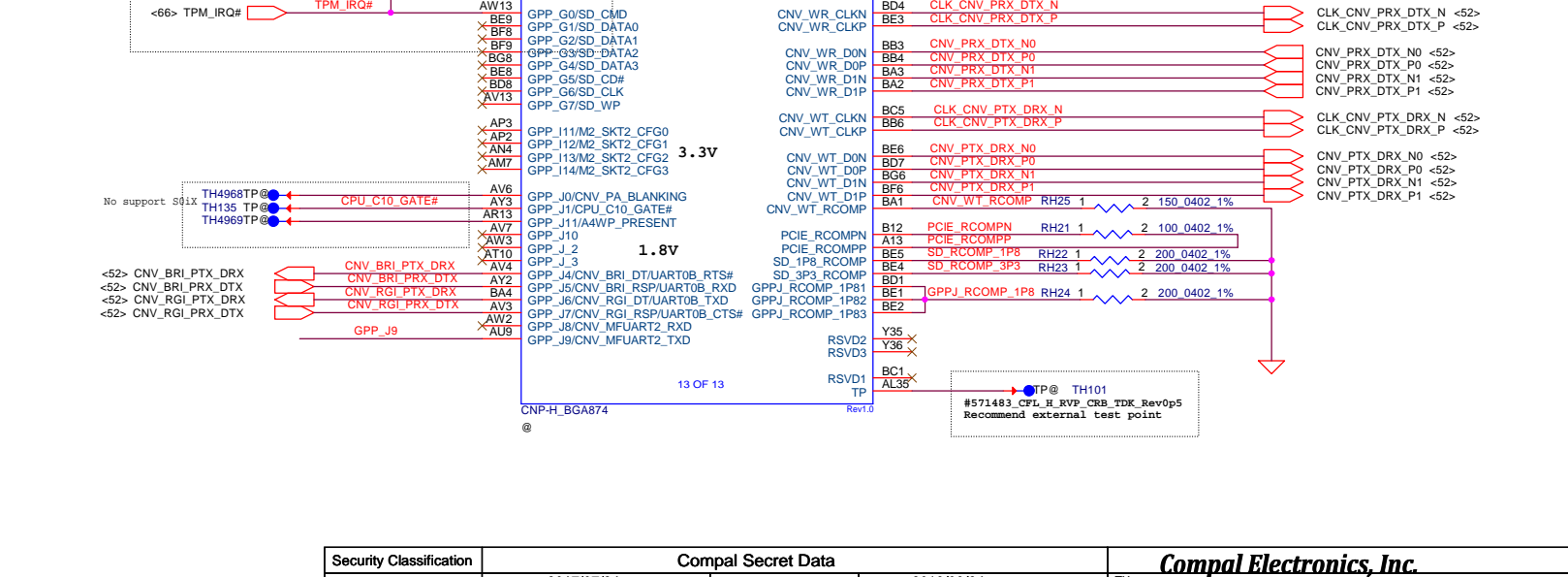
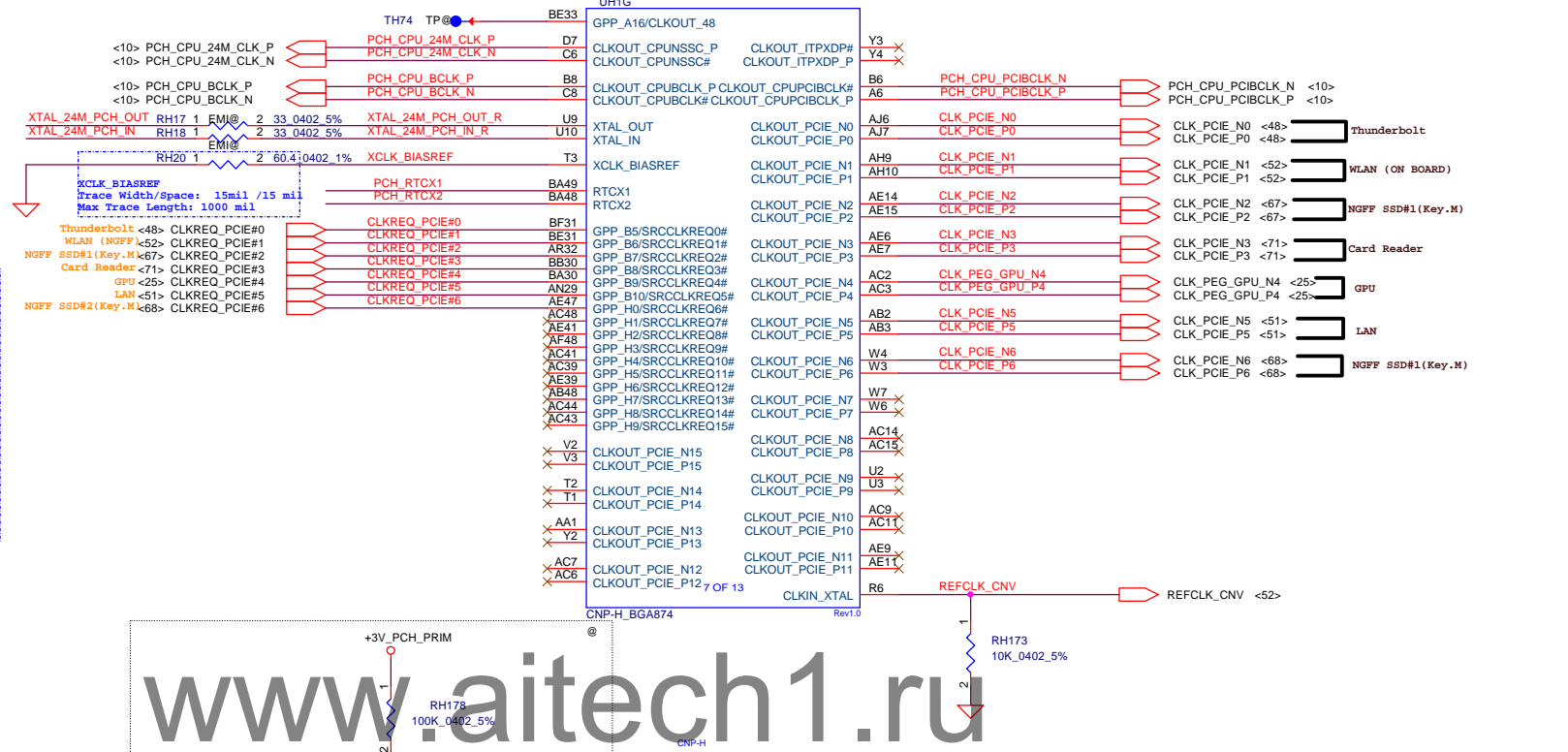
571182-CN-L-PCH-H-EDS-Rev2p2 P.198  
Figure 26-1. Supported PCI Express\* Link Configurations

PCH-H Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 Cycle Router #1				PCIe* Controller #4				PCIe* Controller #5 Cycle Router #3				PCIe* Controller #6 Cycle Router #2				
		Flex I/O Lane #	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
HM370	1x4									RP 9 SSD#1				RP 13				SSD#2 RP 17				TR RP 21				
	1x4 LR									RP 9				RP 13				RP 17				RP 21				
	2x2									RP 9				RP 11				RP 15				RP 19				
	1x2+2x1									RP 9				RP 11				RP 15				RP 19				
	2x1+1x2									RP 12				RP 11				RP 16				RP 15				
QM370	4x1									RP 9				RP 10				RP 11				RP 12				
	1x4									RP 3				RP 9				RP 13				RP 17				
	1x4 LR									RP 3				RP 9				RP 13				RP 17				
	2x2									RP 5				RP 7				RP 11				RP 15				
	1x2+2x1									RP 5				RP 7				RP 8				RP 12				
CM246	2x1+1x2									RP 8				RP 7				RP 5				RP 12				
	4x1									RP 5				RP 6				RP 7				RP 8				
	1x4									RP 3				RP 9				RP 13				RP 17				
	1x4 LR									RP 3				RP 9				RP 13				RP 17				
	2x2									RP 1				RP 3				RP 5				RP 7				
CM248	1x2+2x1									RP 1				RP 3				RP 5				RP 7				
	2x1+1x2									RP 4				RP 3				RP 1				RP 8				
	4x1									RP 1				RP 2				RP 3				RP 4				
	1x4									RP 5				RP 6				RP 7				RP 8				
	1x4 LR									RP 5				RP 6				RP 7				RP 8				

The 30 HSIO lanes on PCH-H supports the following configurations:

- Up to 24 PCIe\* Lanes
  - A maximum of 16 PCIe\* Ports (or devices) can be enabled
  - When a GbE Port is enabled, the maximum number of PCIe\* Ports (or devices) that can be enabled reduces based off the following:
    - max PCIe\* Ports (or devices) = 16 - GbE (0 or 1)
  - PCIe\* Lanes 1-4 (PCIe\* Controller #1), 5-8 (PCIe\* Controller #2), 9-12 (PCIe\* Controller #3), 13-16 (PCIe\* Controller #4), 17-20 (PCIe\* Controller #5), and 21-24 (PCIe\* Controller #6) can be individually configured
- A maximum of 6 SATA Ports (or devices) can be enabled
  - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
  - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
- A maximum of 10 USB 3.1 Ports (or devices) can be enabled
- Up to 6 SATA Lanes
- A maximum of 1 GbE Port (or device) can be enabled
  - Supports up to 3 Remapped (Intel Rapid Storage Technology) PCIe\* storage devices
  - x2 and x4 PCIe\* NVMe SSD
  - x2 Intel Optane\* Memory Device
- See the "PCI Express\* (PCIe\*)" chapter for the PCH PCIe\* Controllers, configurations, and lanes that can be used for Intel Rapid Storage Technology PCIe\* storage support
- For unused SATA/PCIe\* Combo Lanes, Flex I/O Lanes that can be configured as PCIe\* or SATA, the lanes must be statically assigned to SATA or PCIe\* via the SATA/PCIe\* Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel Flash Image Tool (FIT) tool.





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				Date:	Friday, September 28, 2018	Sheet 15 of 100





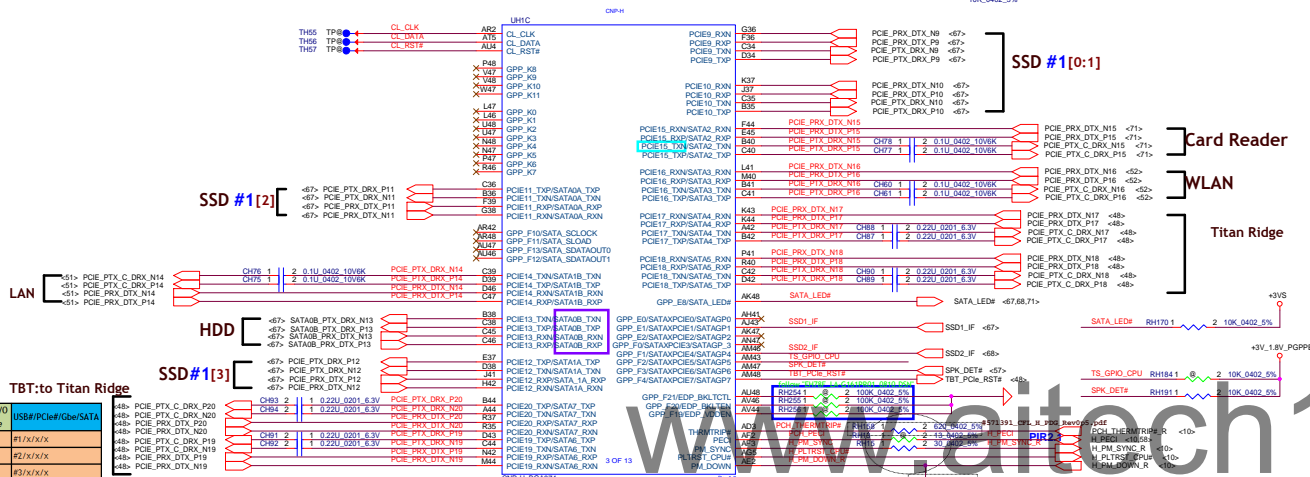
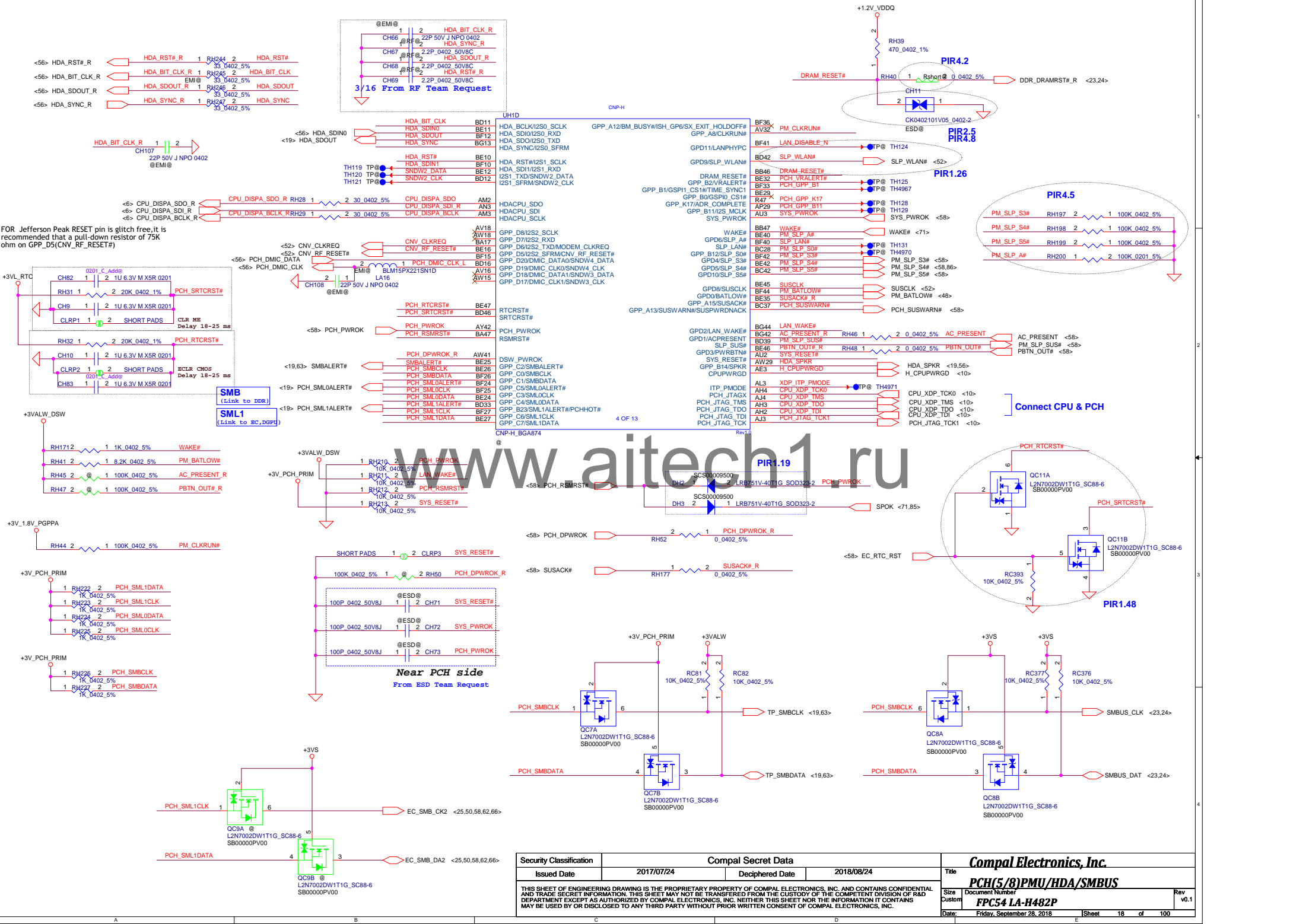


Figure 26-1. Supported PCIE Express® Link Configurations																																
PCB# Details		PCB# Controller #1				PCB# Controller #2				PCB# Controller #3				PCB# Controller #4				PCB# Controller #5				PCB# Controller #6										
Flex I/O Lane #		Cycle Router #1				Cycle Router #2				Cycle Router #3				Cycle Router #4				Cycle Router #5				Cycle Router #6										
		6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34		
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
																												</				



FOR Jefferson Peak RESET pin is glitch free, it is recommended that a pull-down resistor of 75K ohm on GPP\_D5(CNV\_RF\_RESET#)

SMB (link to DDR)  
SML1 (link to EC, DGP1)

Near PCH side  
From ESD Team Request

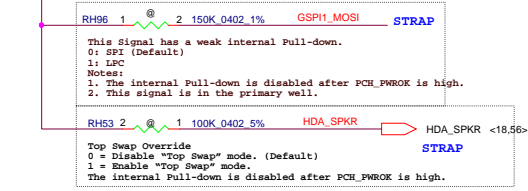
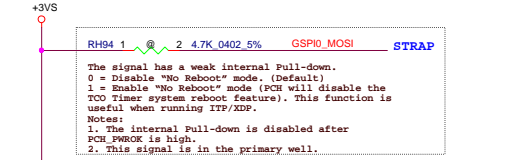
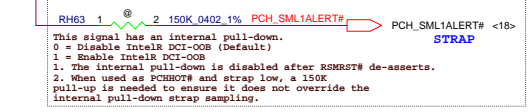
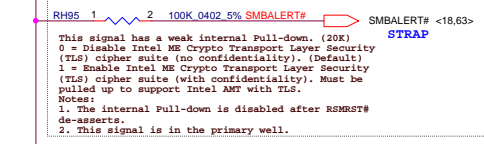
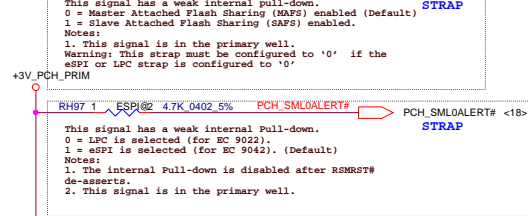
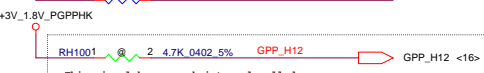
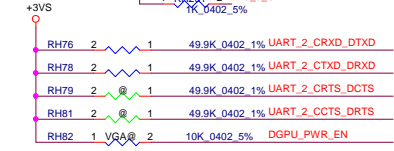
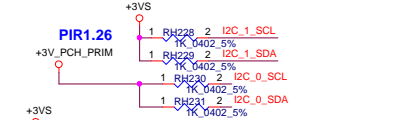
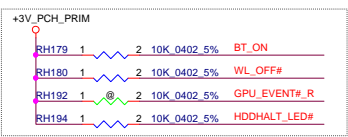
Near PCH side  
From RF Team Request

Near PCH side  
From ESD Team Request

Near PCH side  
From RF Team Request

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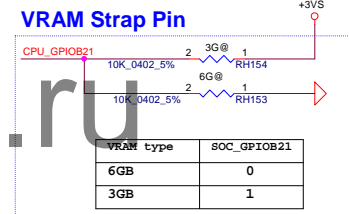
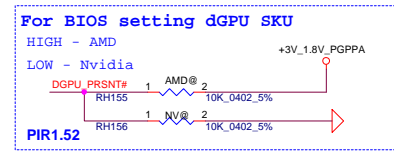
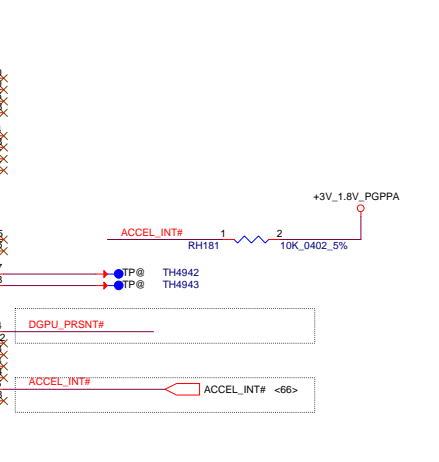
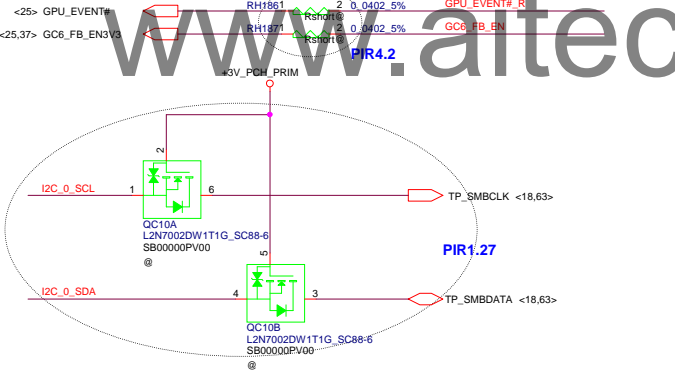
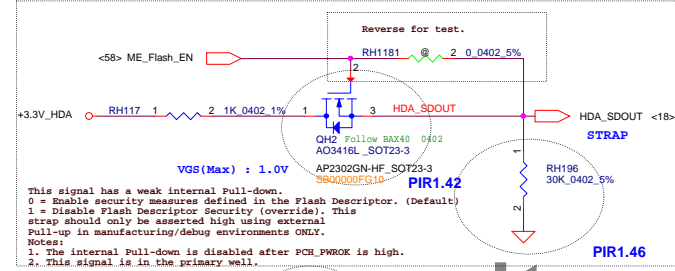
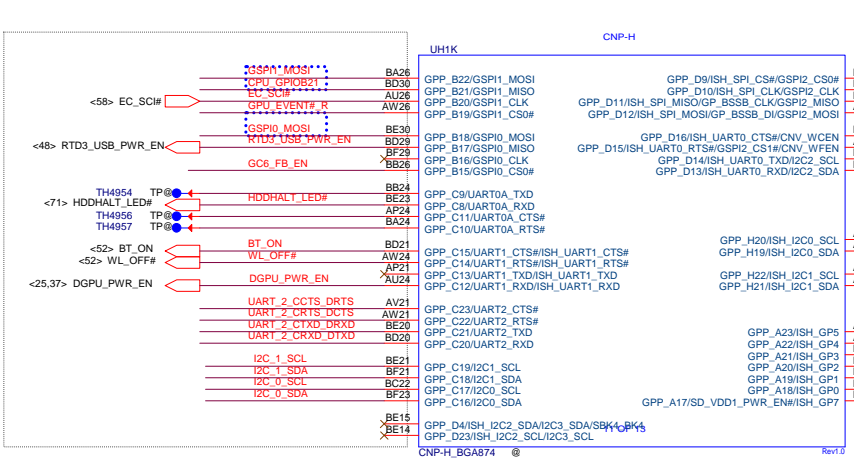
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PCH(5/8)PMU/HDA/SMBUS		Document Number	
FPC54 LA-H482P		Rev	
Date: Friday, September 28, 2018		Sheet 18 of 100	



SCI capability is available on all GPIOs  
PCH GPIOs that can be routed to generate SMI# or NMI:  
• GPP\_B14, GPP\_B20, GPP\_B23  
• GPP\_C123:221  
• GPP\_D14:0  
• GPP\_E16:0  
• GPP\_I13:0  
• GPP\_G17:0 (support SMI# only).

The voltage of all GPIO pads in each GPP group is determined by the voltage supplied to the group (either 3.3V or 1.8V) except for GPP\_I and GPP\_G group, (which are 3.3V only), and GPP\_J group (which is 1.8V only).

All GPIOs have programmable internal pull-up/pull-down resistors which are off by default.  
The internal pull-up/pull-down for each GPIO can be enabled by BIOS programming.

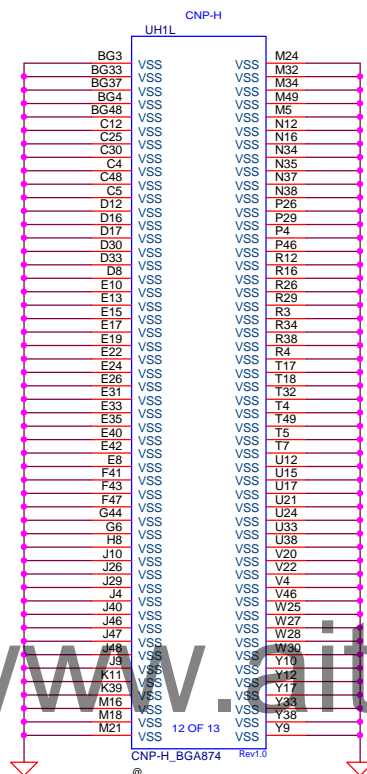


For Debug Port80/RMT/MMA

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					Size	
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					v0.1	
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# Interleaved Memory

( 4 mm )

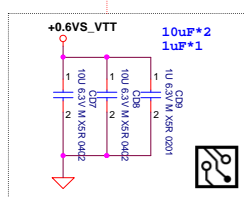
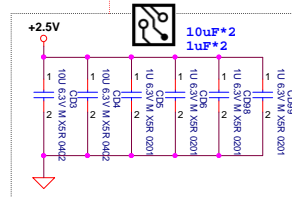
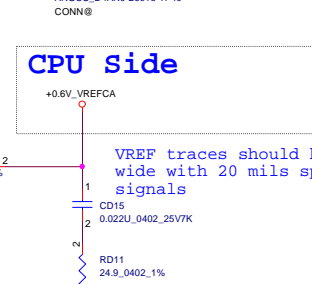
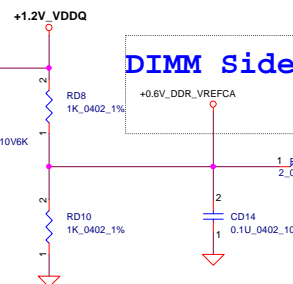
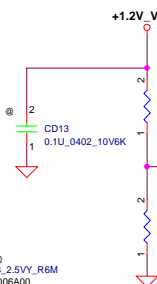
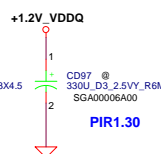
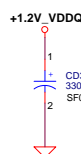
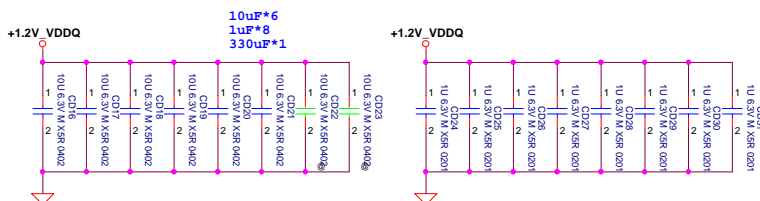
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**M**

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<7> DDR_M0_D[16..31]		
<7> DDR_M0_D[32..47]		
<7> DDR_M0_D[48..63]		

[illegible]

Layout Note:  
Place near JDIMM1.258

[illegible][illegible]

For ECC DIMM

PLACE NEAR TO SODIMM

## DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

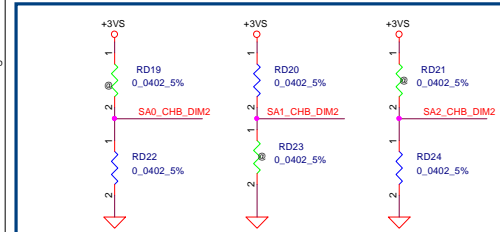
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				Date:	Friday, September 28, 2018	Sheet 23 of 100

# CHANNEL-B

17.3"=>Reverse TYPE ( 8 mm)

## Interleaved Memory

TOP: JDIMM2 CONN Non-ECC DIMM

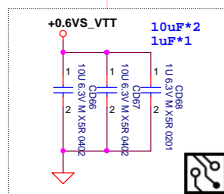
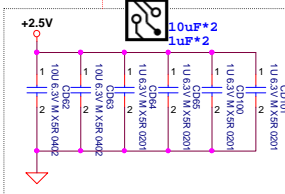


PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

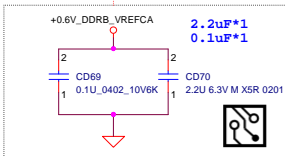
SPD ADDRESS FOR CHANNEL B :  
WRITE ADDRESS: 0XA4  
READ ADDRESS: 0XA3  
SA0 = 0; SA1 = 1; SA2 = 0.  
DDR4 POR OPERATING SPEED: 1867 MT/S  
STRETCH GOAL IS 2133 MT/S

Layout Note:  
Place near JDIMM2.257,259

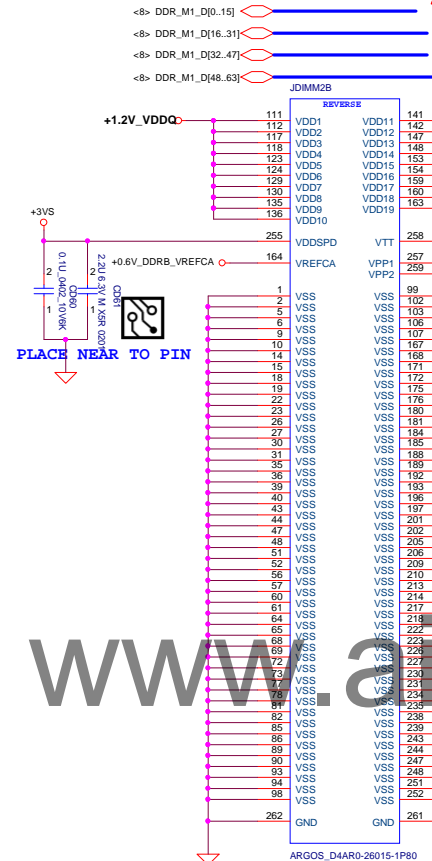
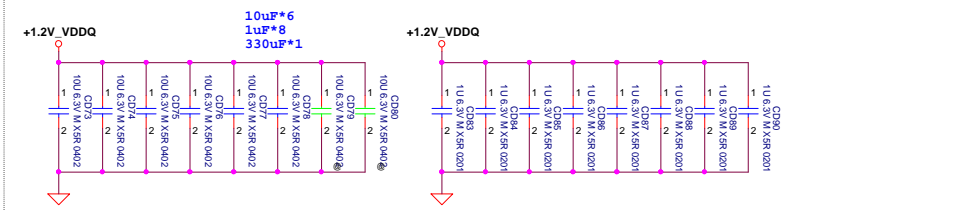
Layout Note:  
Place near JDIMM2.258



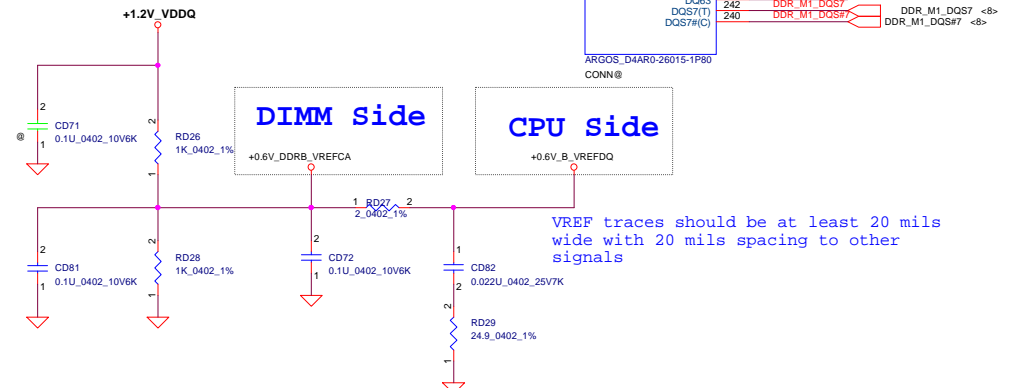
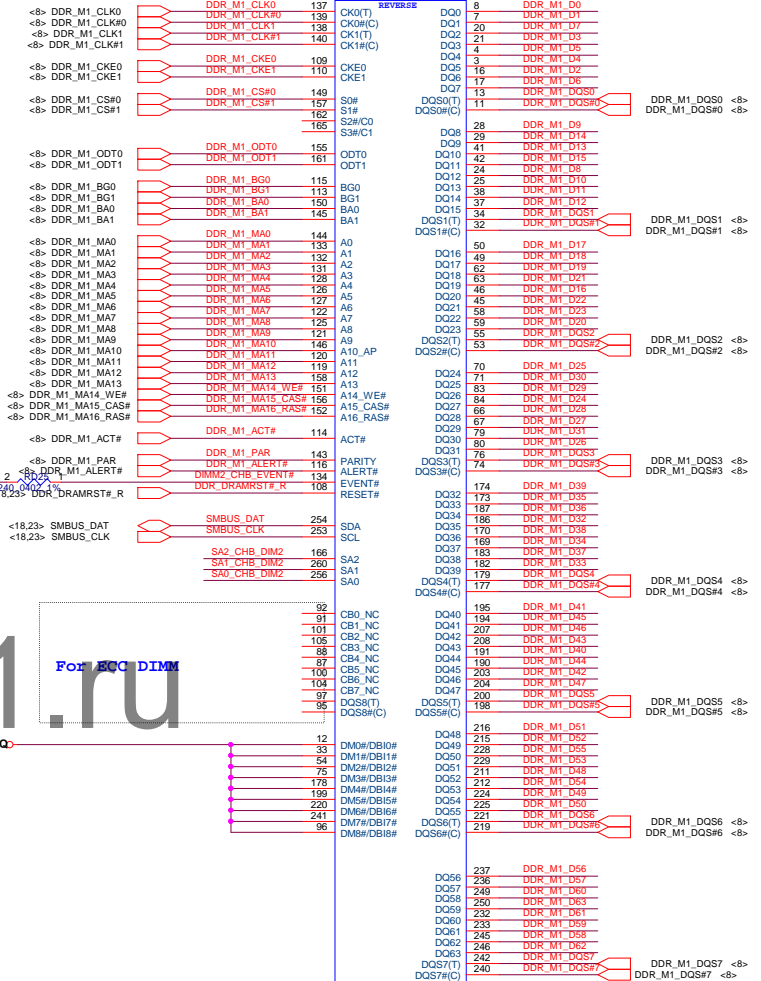
Layout Note:  
PLACE THE CAP WITHIN 200 MILS  
FROM THE JDIMM2



Layout Note:  
Place near JDIMM2



PLACE NEAR TO PIN

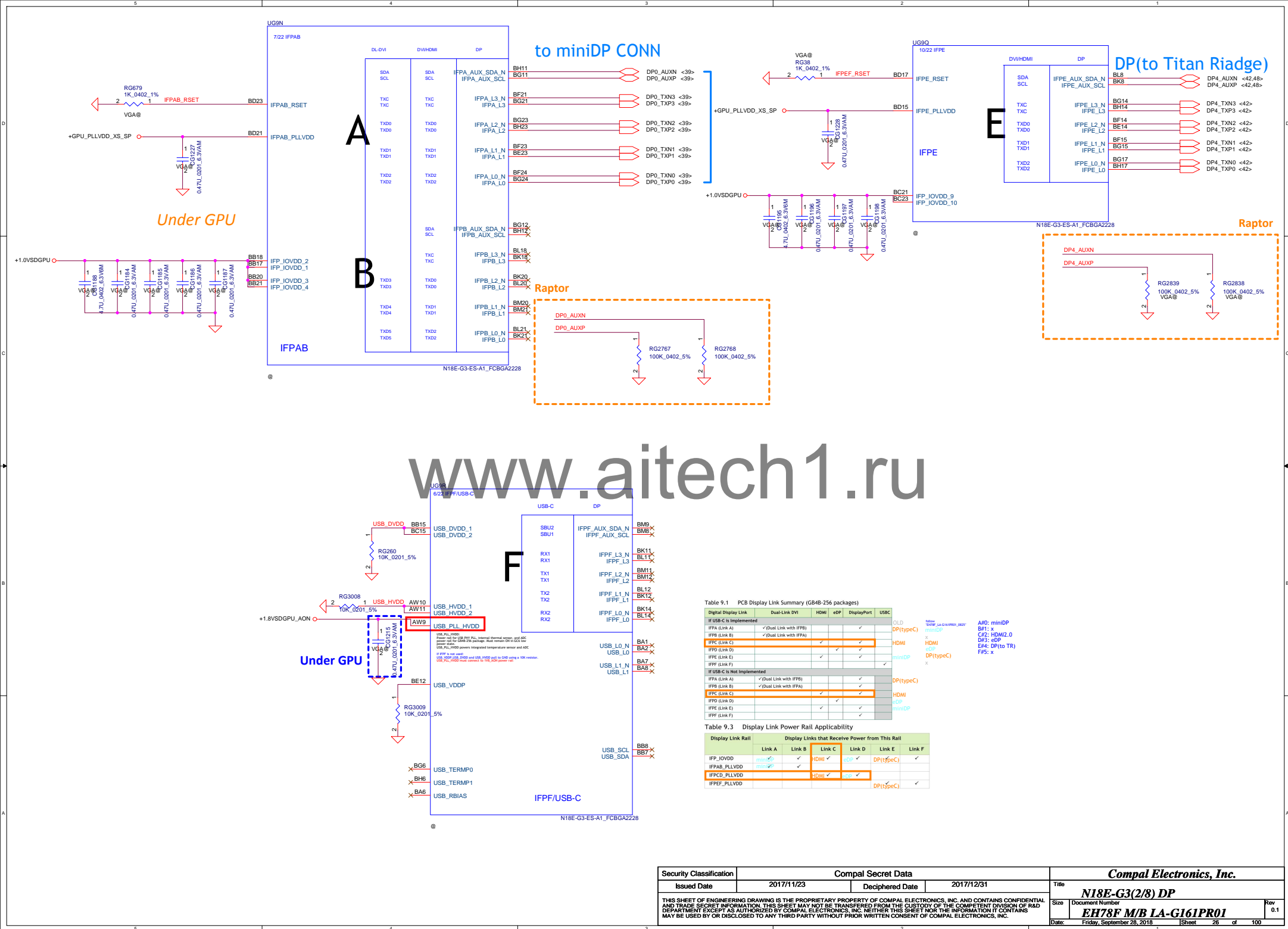


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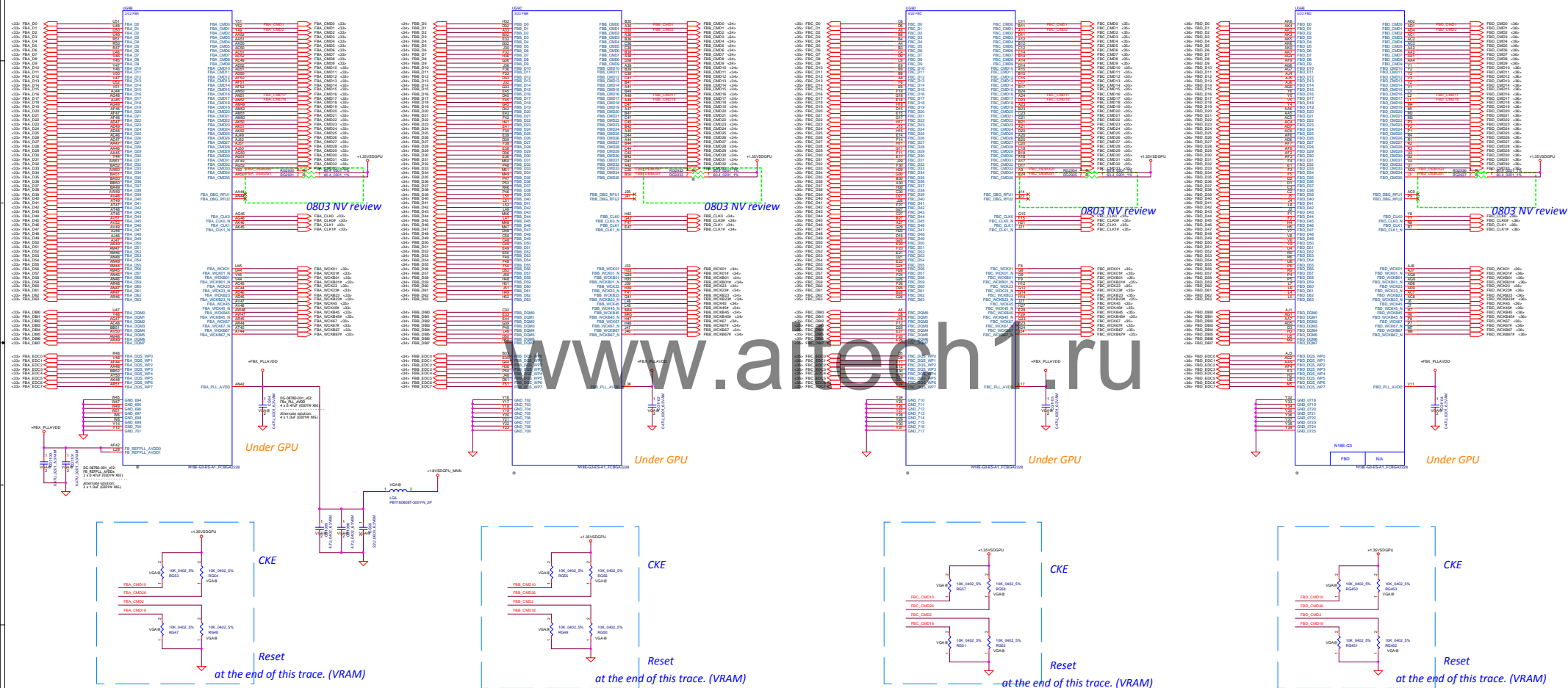
2,58,66,67,68,71> PLT\_RST#











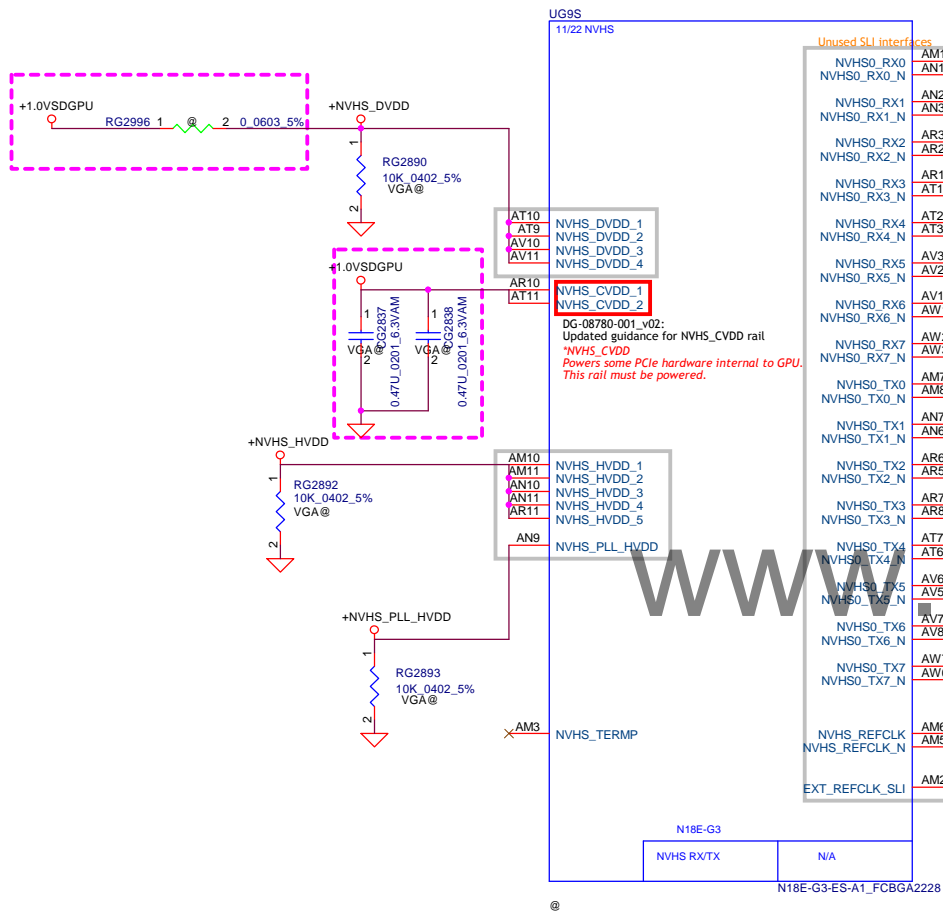








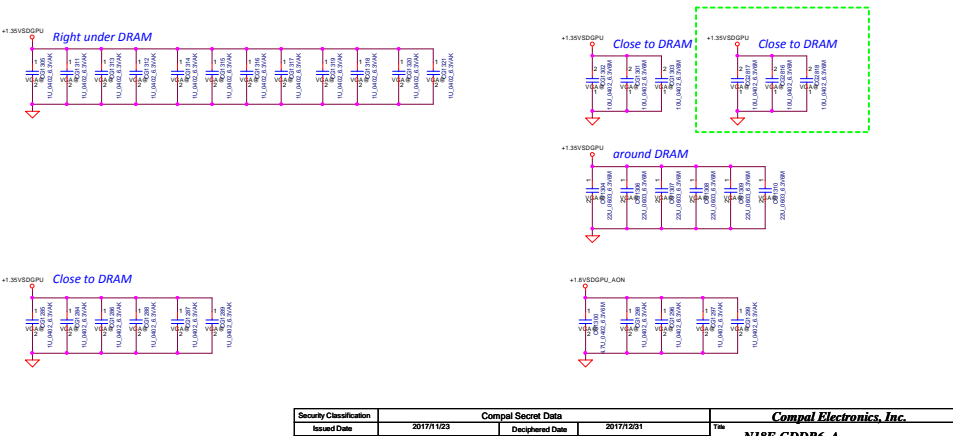
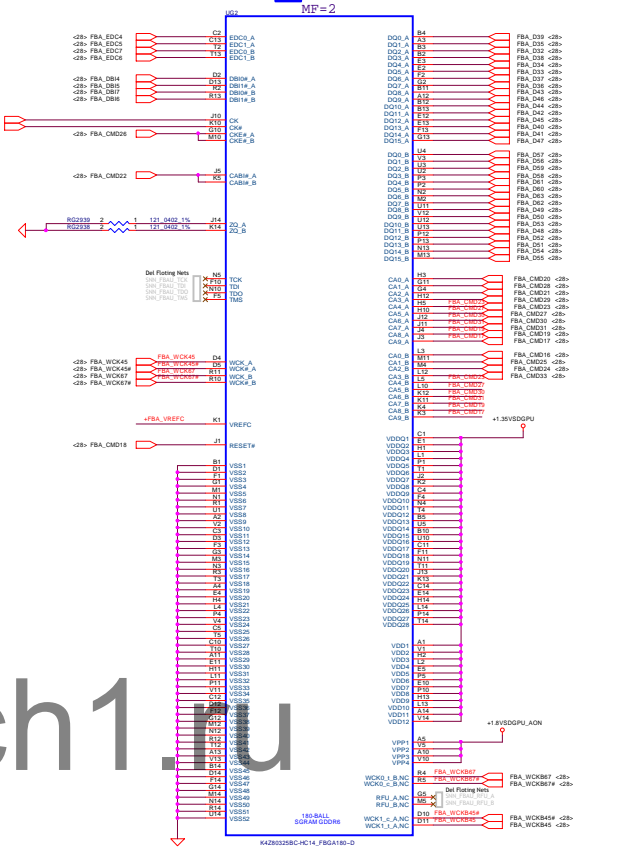
Pull down NVHS\_DVDD, NVHS\_CVDD, NVHS\_HVDD, NVHS\_PLL\_HVDD rails to GND with 10K Resistor



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				Rev	0.1
				EH78F M/B LA-G161PR01	

**1\_A#1**

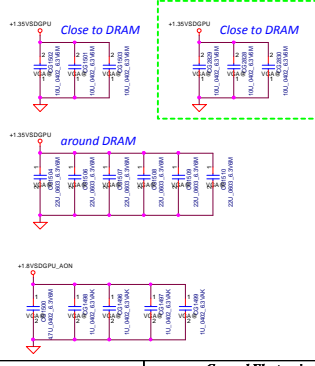
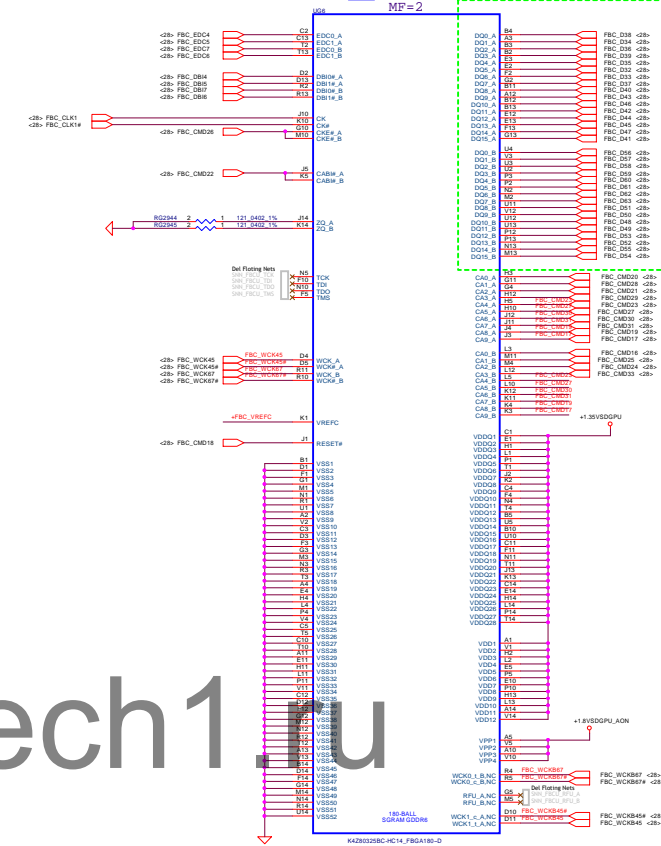


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## 5 C#



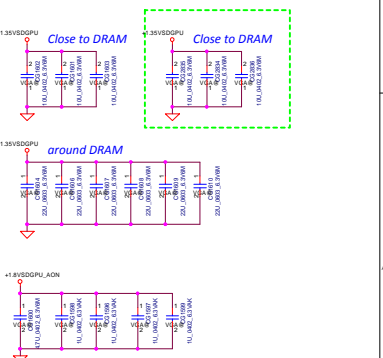
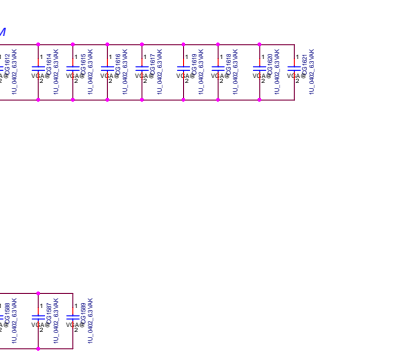
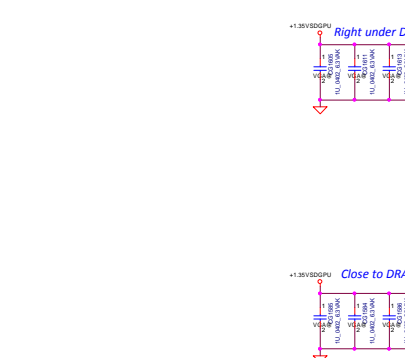
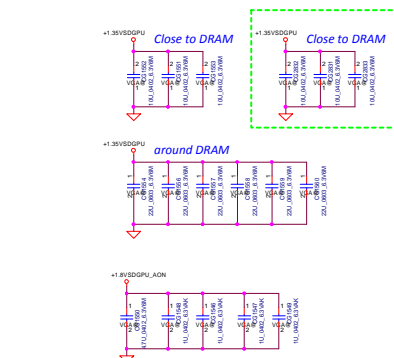
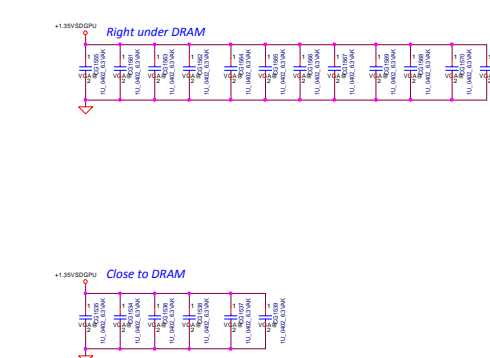
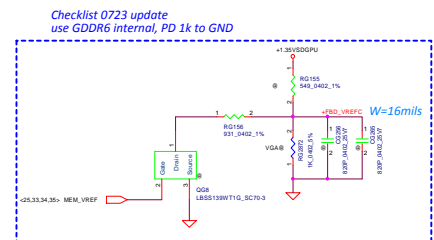
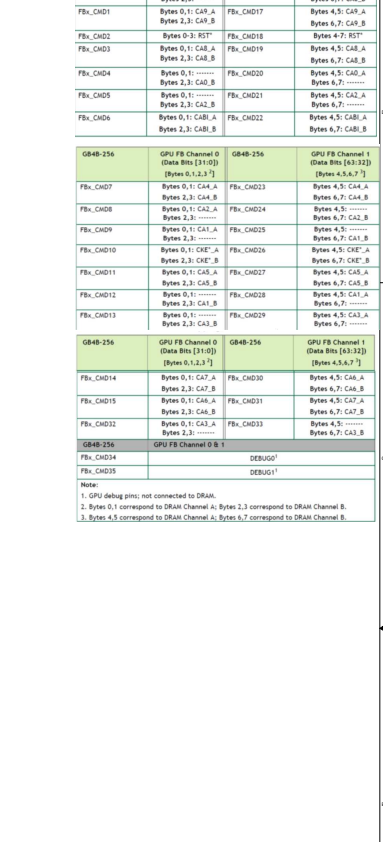
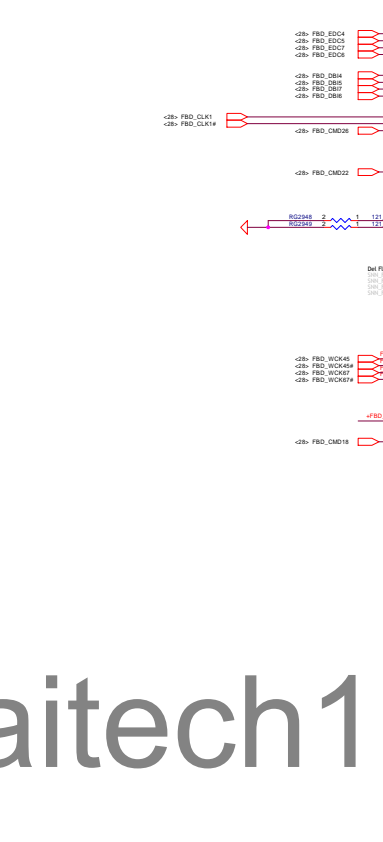
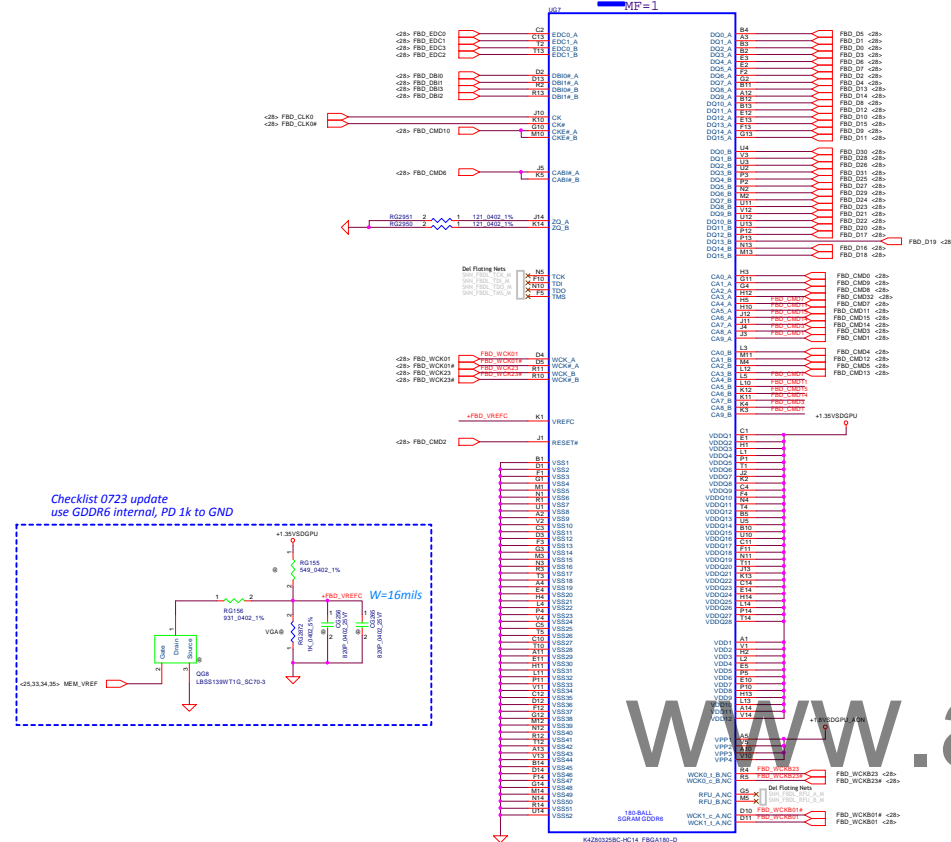
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Fb_C0D0	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D16	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D1	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D17	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D2	Bytes 0:3: H0T	Fb_C0D18	Bytes 4:7: CA0_A
Fb_C0D3	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D19	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D4	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D20	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D5	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D21	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D6	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D22	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
GR48-256	GPU FB Channel 0 (Data Bits [31:0])  (Bytes 1.2,3,4)	GR48-256	GPU FB Channel 1 (Data Bits [63:32])  (Bytes 4.5,6,7)
Fb_C0D7	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D23	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D8	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D24	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D9	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D25	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D10	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D26	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D11	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D27	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D12	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D28	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D13	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D29	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
GR48-256	GPU FB Channel 0 (Data Bits [31:0])  (Bytes 1.2,3,4)	GR48-256	GPU FB Channel 1 (Data Bits [63:32])  (Bytes 4.5,6,7)
Fb_C0D14	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D30	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D15	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D31	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
Fb_C0D16	Bytes 0:1: CA0_A Bytes 2: CA0_B	Fb_C0D32	Bytes 4:5: CA0_A Bytes 6:7: CA0_B
GR48-256	GPU FB Channel 0 B I		
Fb_C0D33A		DEBUG0 <sup>1</sup>	
Fb_C0D33B		DEBUG1 <sup>1</sup>	

Note:

1. GPU debug pins; not connected to DRAM.
2. Bytes 0:1 correspond to DRAM Channel A, Bytes 2:3 correspond to DRAM Channel B.
3. Bytes 4:5 correspond to DRAM Channel A, Bytes 6:7 correspond to DRAM Channel B.

8\_D#2

7\_D#1

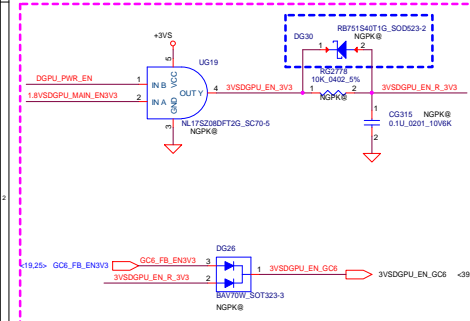


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Rev	1	Rev	1	Rev	1
Rev	1	Rev	1	Rev	1
Rev	1	Rev	1	Rev	1

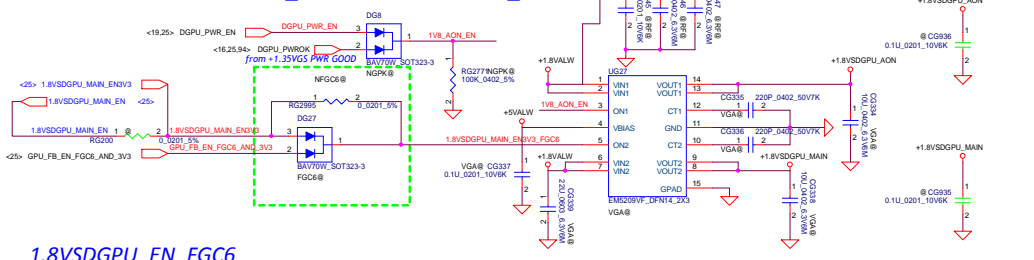


No Reserved NV Sequence IC: SILEGO GreenPAK  
SA0000B9H00, S IC SLG4U41989VTR STQFN 20P LOGIC SOC

## +3VS/+3VSDGPU



## +1.8VALW to +1.8VSDGPU\_AON & +1.8VSDGPU\_MAIN

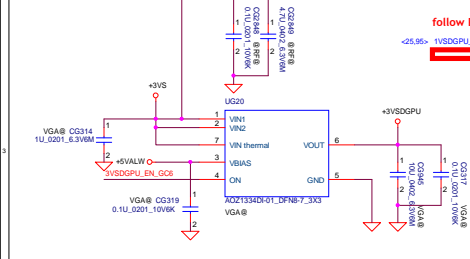


### 1.8VSDGPU\_EN\_FGC6

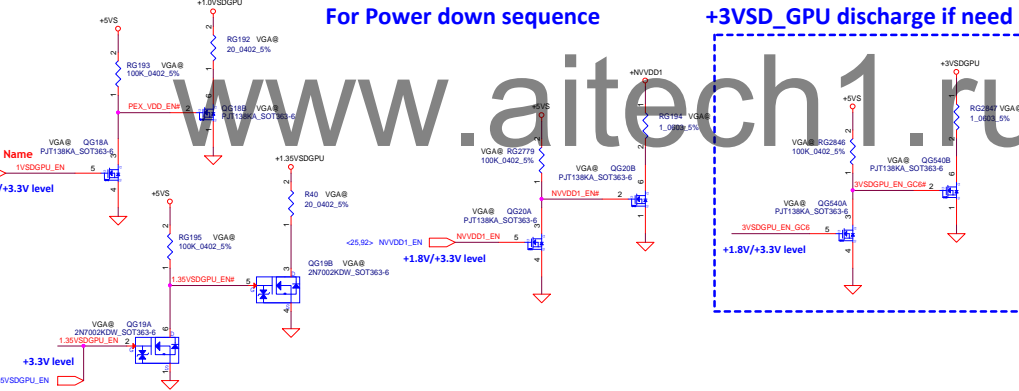
For Power down sequence

+3VSD\_GPU discharge if need

## 3VSDGPU\_EN\_GC6

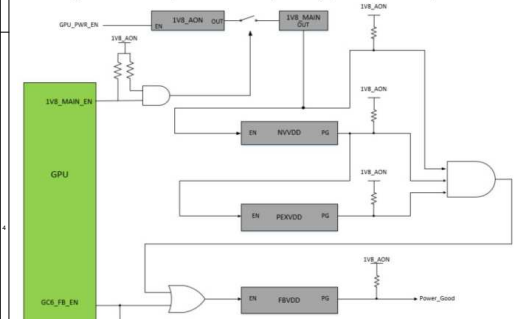


follow PWR Net Name  
+1.8V/+3.3V level

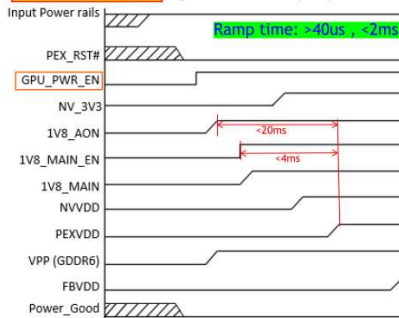


## DG-08780-001\_v02

Figure 5.5 Example of Power Sequencing (GPU rails shown)

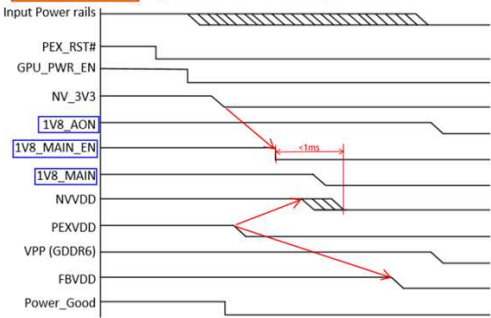


## DG-08780-001\_v02 Figure 5.6 Power-Up Sequence



## DG-08780-001\_v02

Figure 5.7 Power-Down Sequence

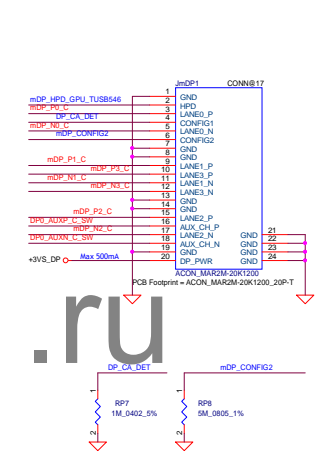
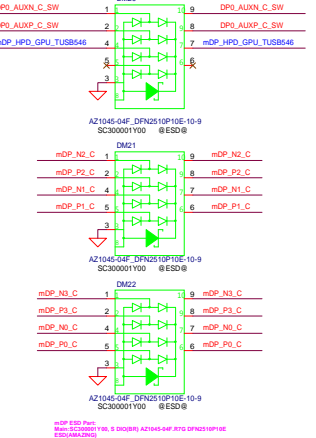
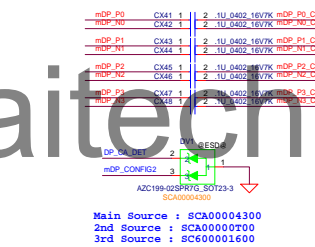
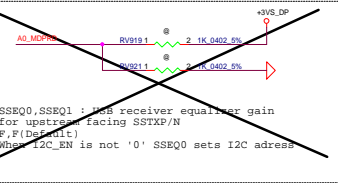
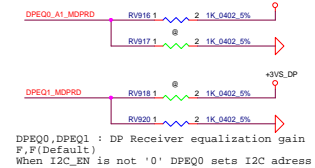
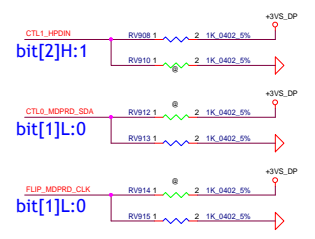




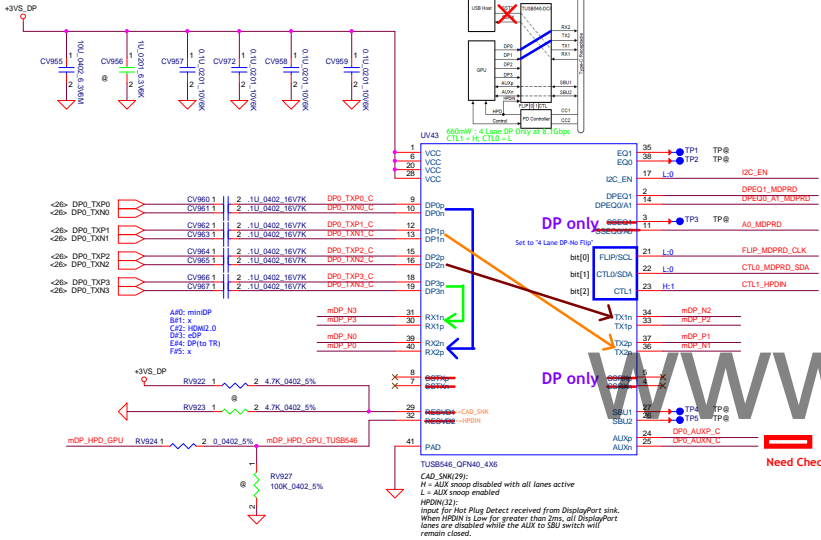
I2C Programming or pin strap programming select.  
I2C is only disable when this pin is '0'  
0 : Pin Strap(I2C disable)(Default)  
R : TI test mode(I2C enable at 3.3V)  
F : I2C enabled at 1.8V  
1 : I2C enabled at 3.3V



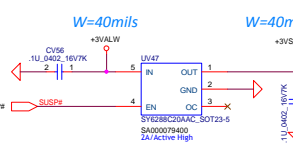
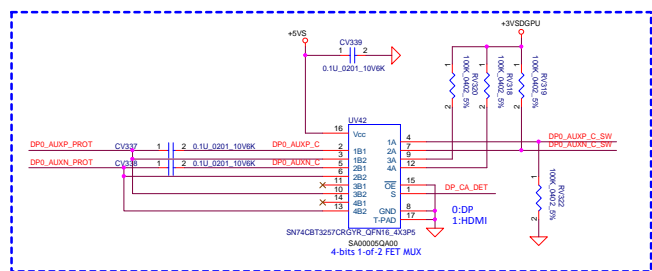
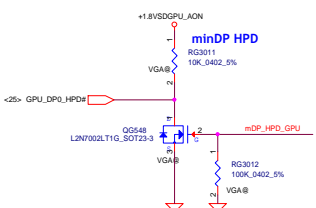
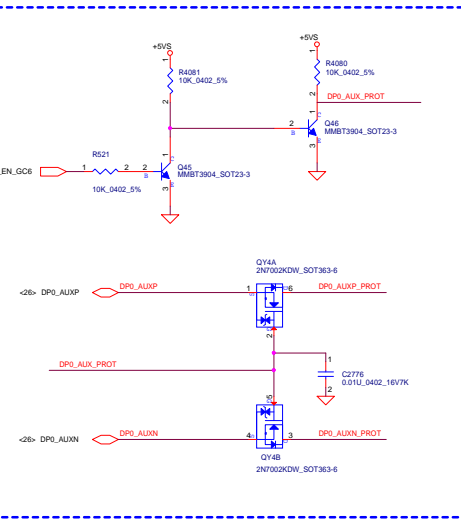
I2C Programming or pin strap programming select.  
I2C is only disable when this pin is '0'  
0 : Pin Strap(I2C disable)(Default)  
R : TI test mode(I2C enable at 3.3V)  
F : I2C enabled at 1.8V  
1 : I2C enabled at 3.3V



### Simplified Schematics



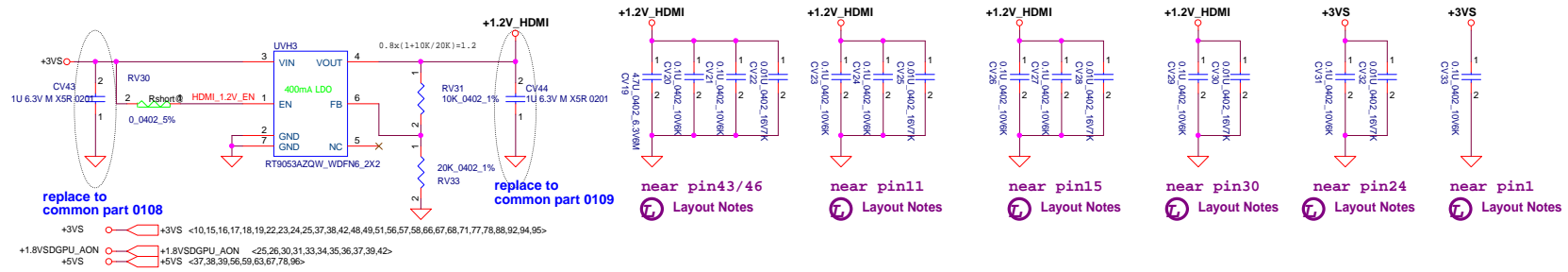
## DP++ and isolated circuit



OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1 (0:DP)
L	H	B2	A=B2 (1:HD)
H	X	Z	NC

```
0921 change souce to +3VALW, CTRL to SUSP#
```

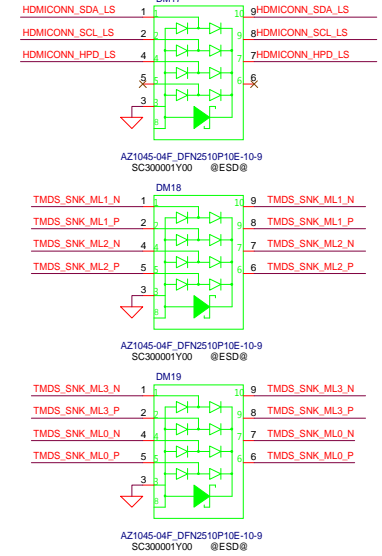
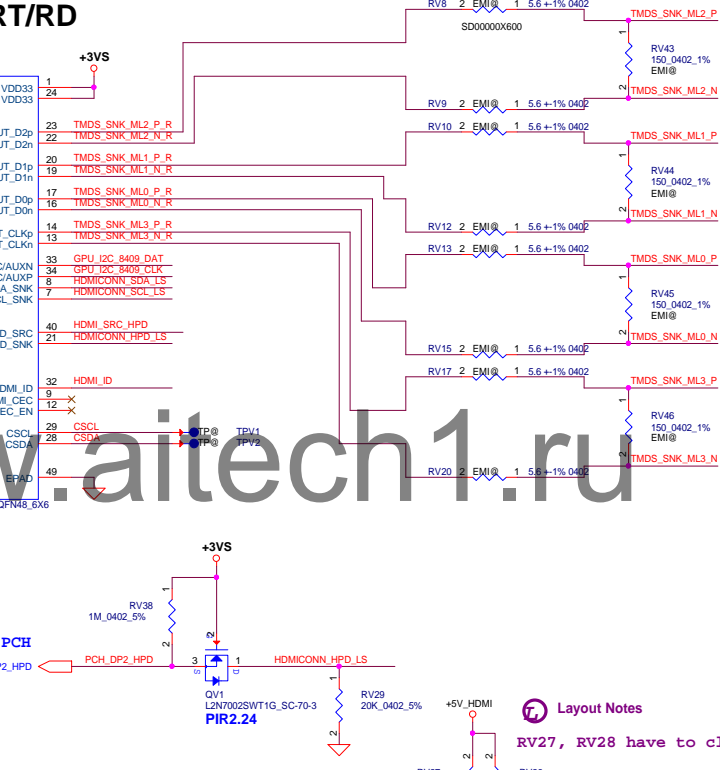
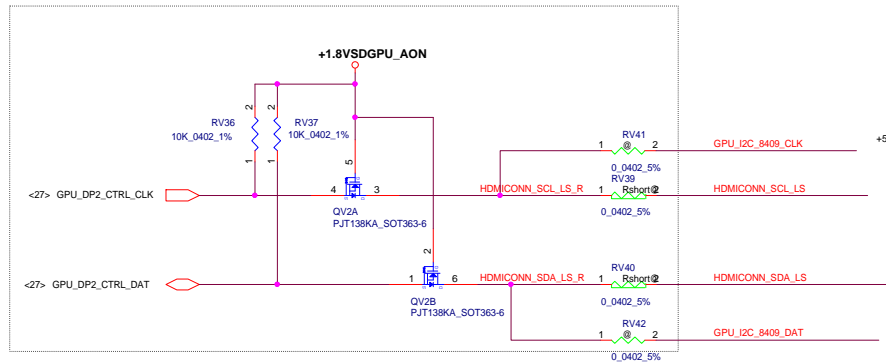
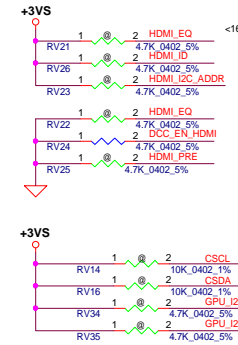
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## HDMI2.0 RT/RD

DP: miniDP  
H0: #1  
H1: #2  
H2: #3  
H3: #4  
H4: #5  
H5: #6

GPU(IFP#C)



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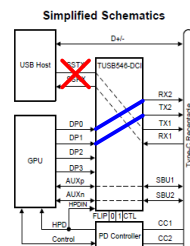
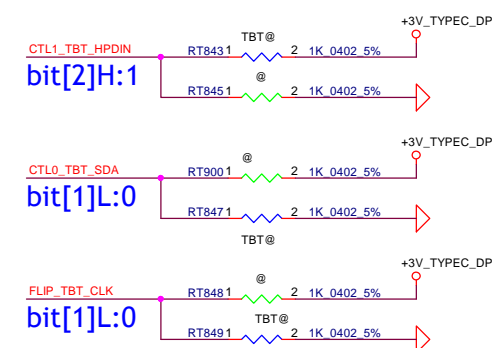
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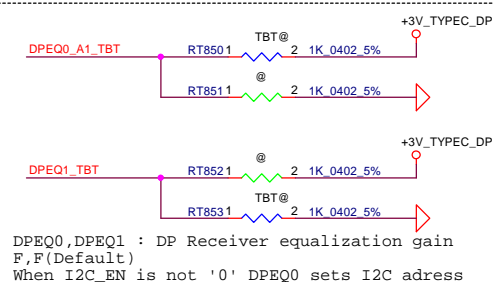


**I2C = pin mode (I2C disable)**

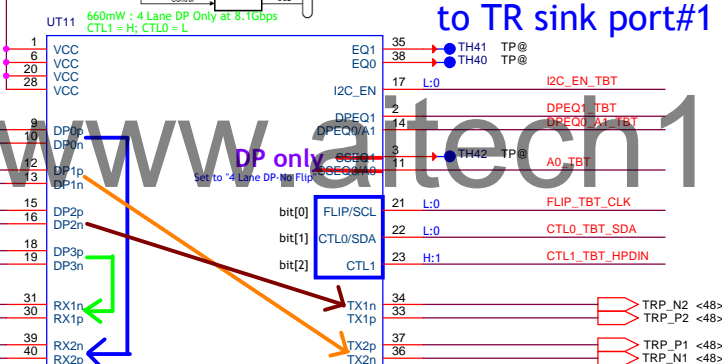
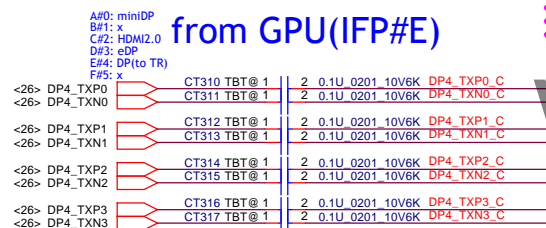
I2C Programming or pin strap programming select  
I2C is only disable when this pin is '0'  
0 : Pin Strap(I2C disable)(Default)  
R : TI test mode(I2C enable at 3.3V)  
F : I2C enabled at 1.8V  
1 : I2C enabled at 3.3V



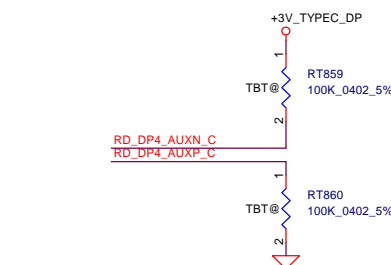
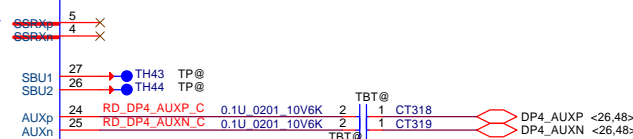
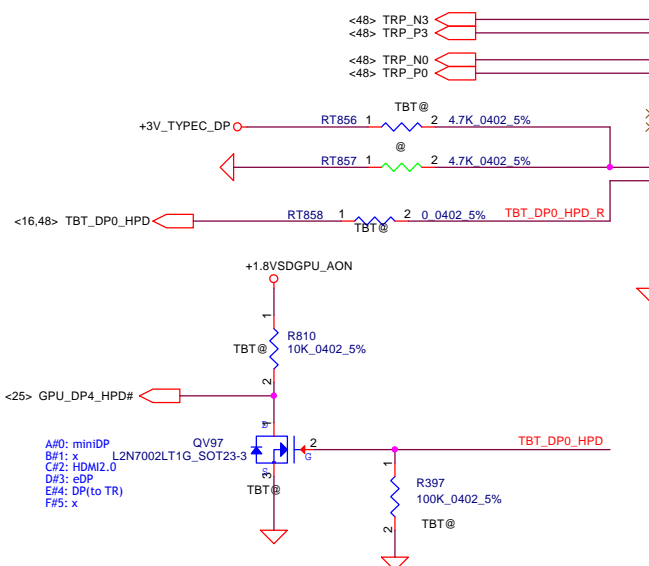
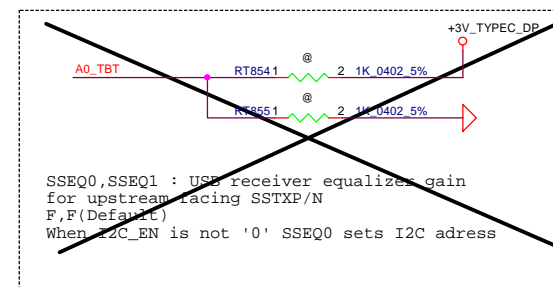
to TR sink port#1



from GPU(IFP#E)



DP only



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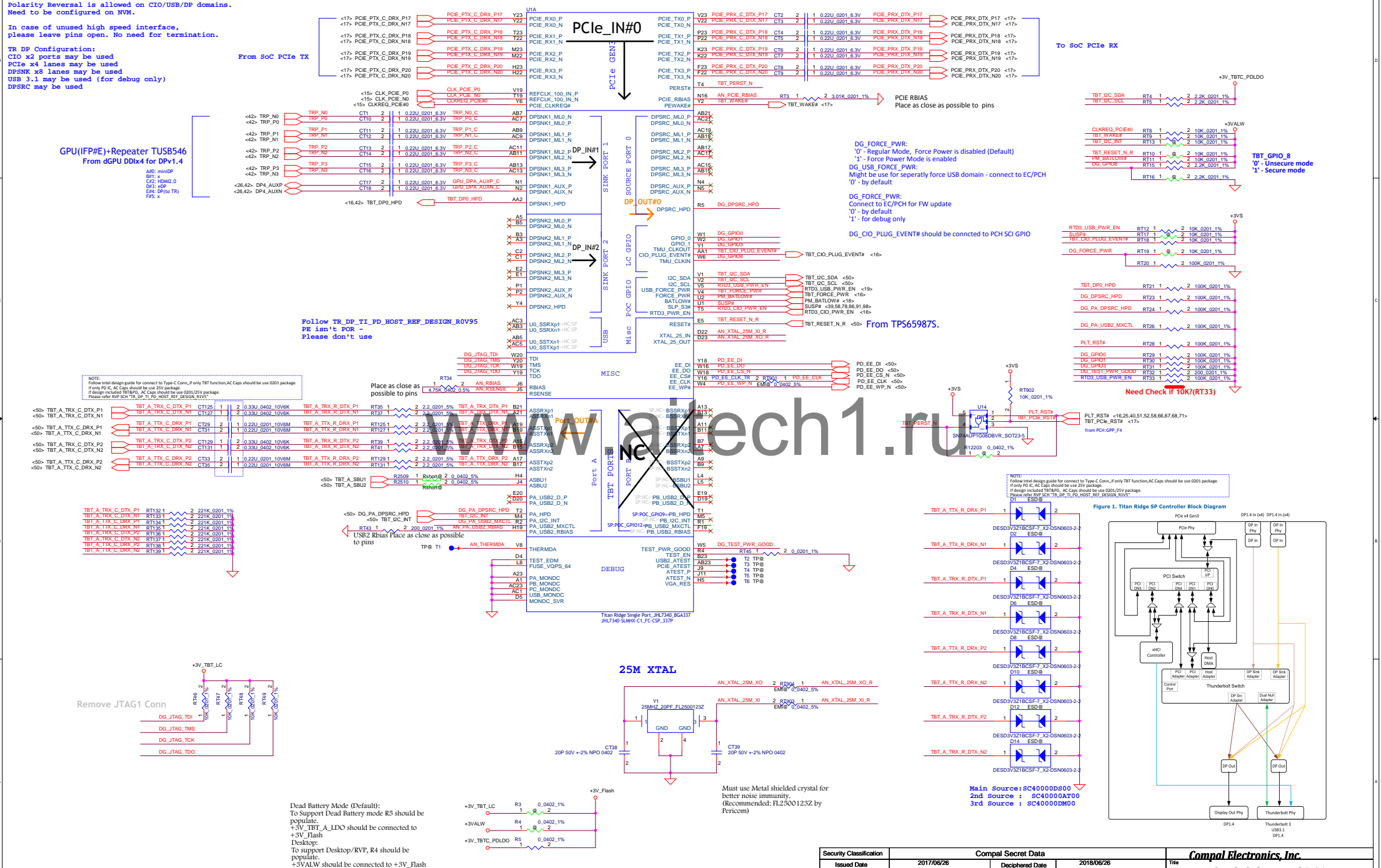


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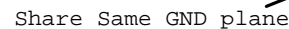
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				Date	Friday, September 28, 2018
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**SE**  
(Single Port)

```
TR DP Configuration:
CIO x2 ports may be used
PCIe x4 lanes may be used
DPSNK x8 lanes may be used
USB 3.1 may be used (for debug only)
DPSRC may be used
```

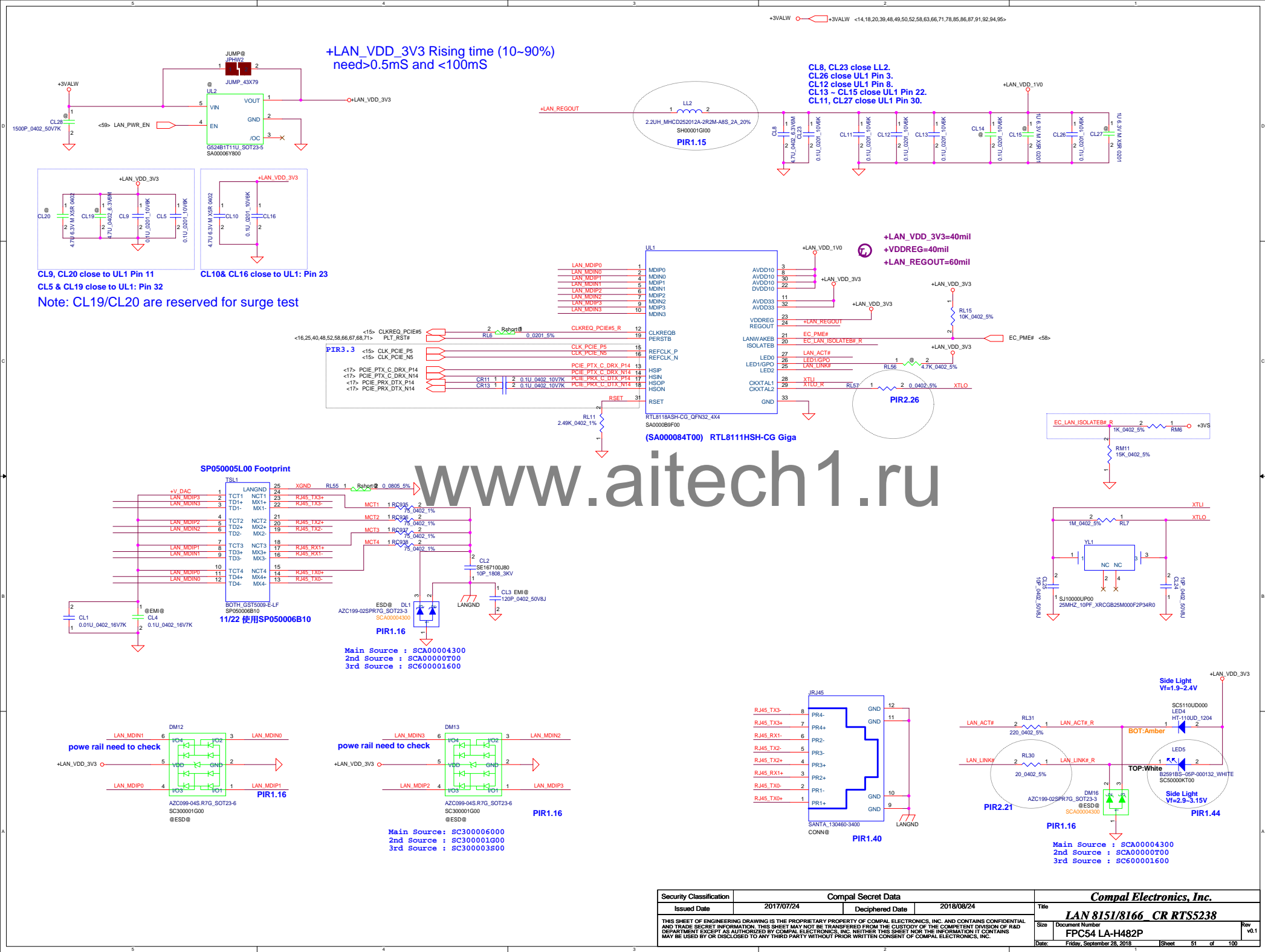


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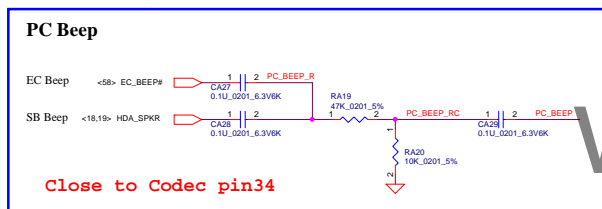
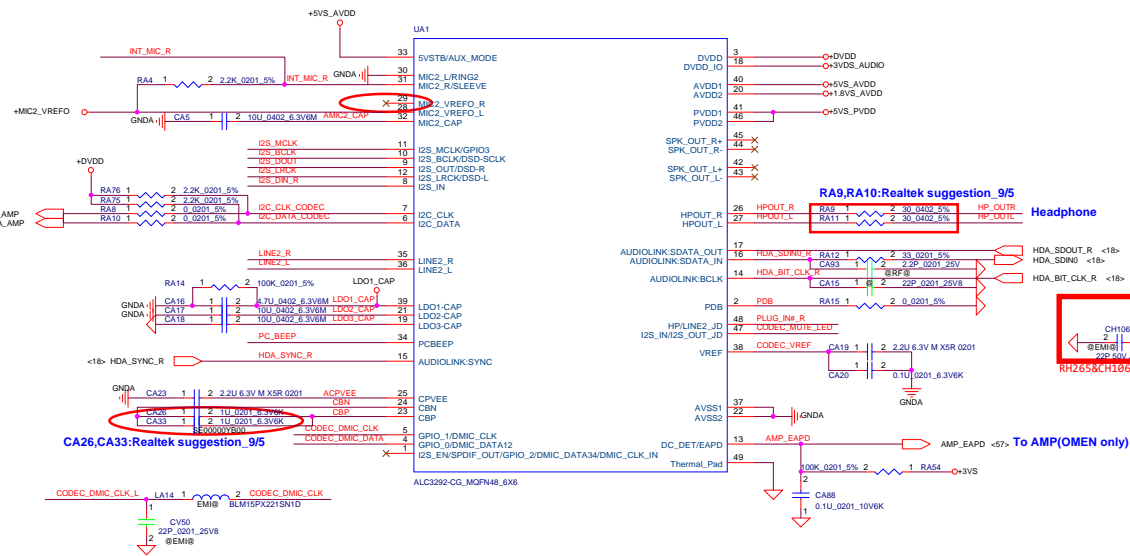
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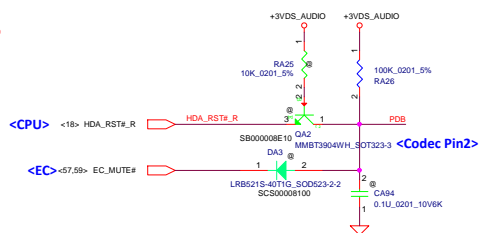
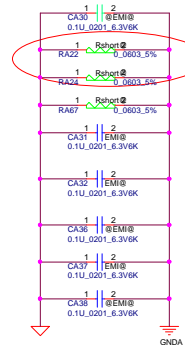
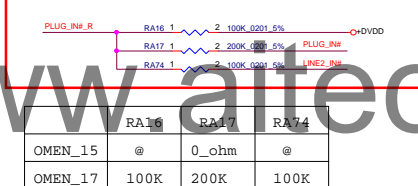
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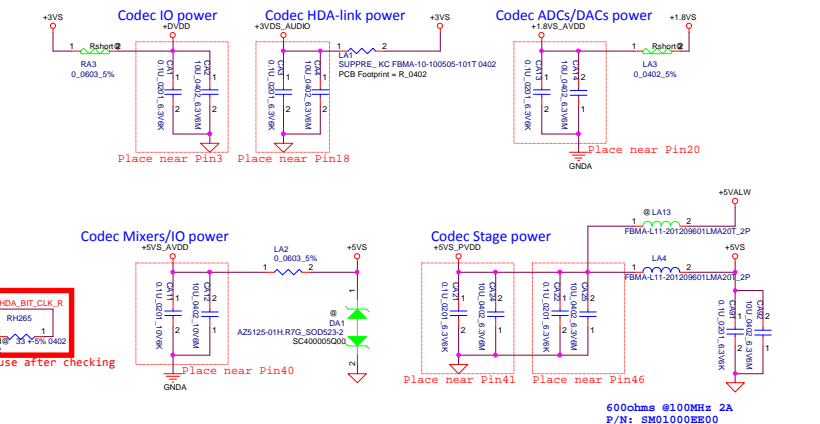
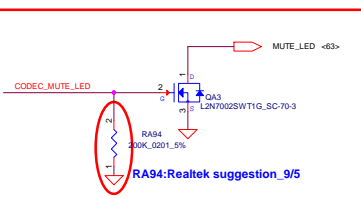
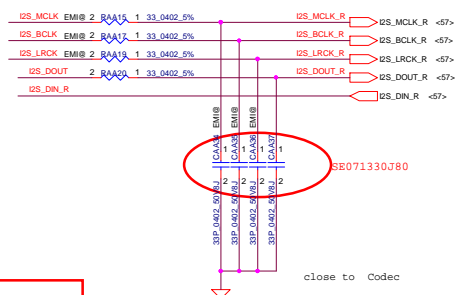
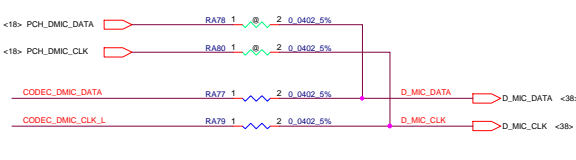
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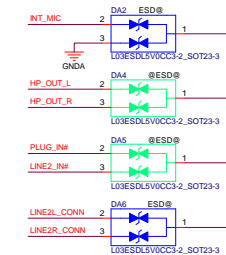
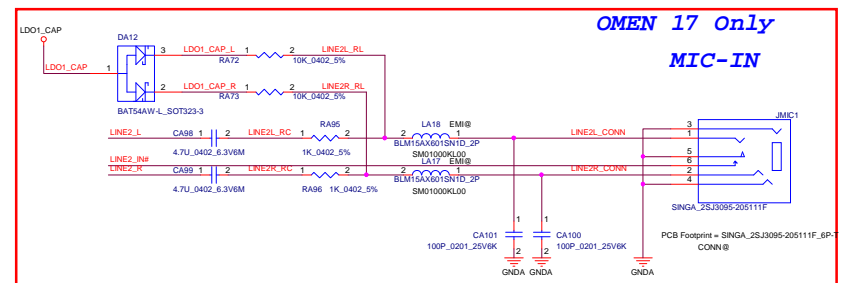
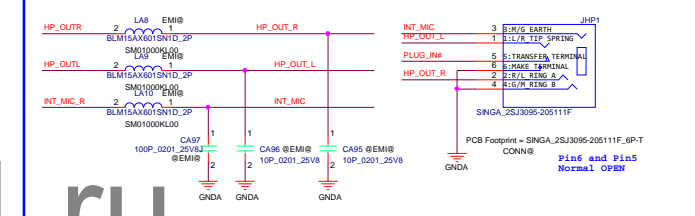
## Jack Detect



Camera DMIC select



Combo Jack



DA2,DA4~DA6  
Main Source : SCA00002900  
2nd Source : SCA00001A00  
3rd Source : SCA00000T00



**Headphone Jack Type**

Audio jack must be plastic without conductive coatings (no chrome).<sup>4</sup>

**Individual Audio Jack for Headphone & Microphone**

**Audio jack pin configuration:**

**Combo Jack (Headset / Headphone compatible):**

Tip = Left

1st ring = Right

2nd ring = Ground  
Sleeve = Mono microphone

Sleeve = Mono microphone<sup>43</sup>

**Microphone Jack (Milos/Santorini)**

Tip = Left

Ring = Right

Sleeve = Ground

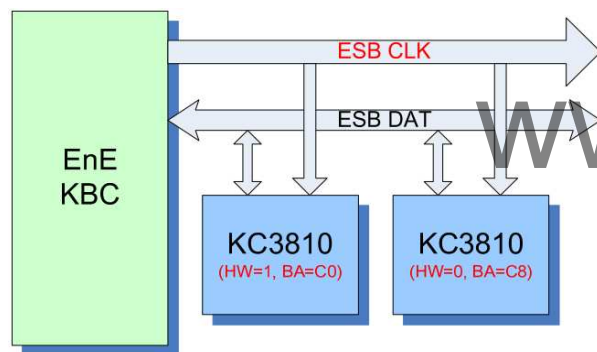
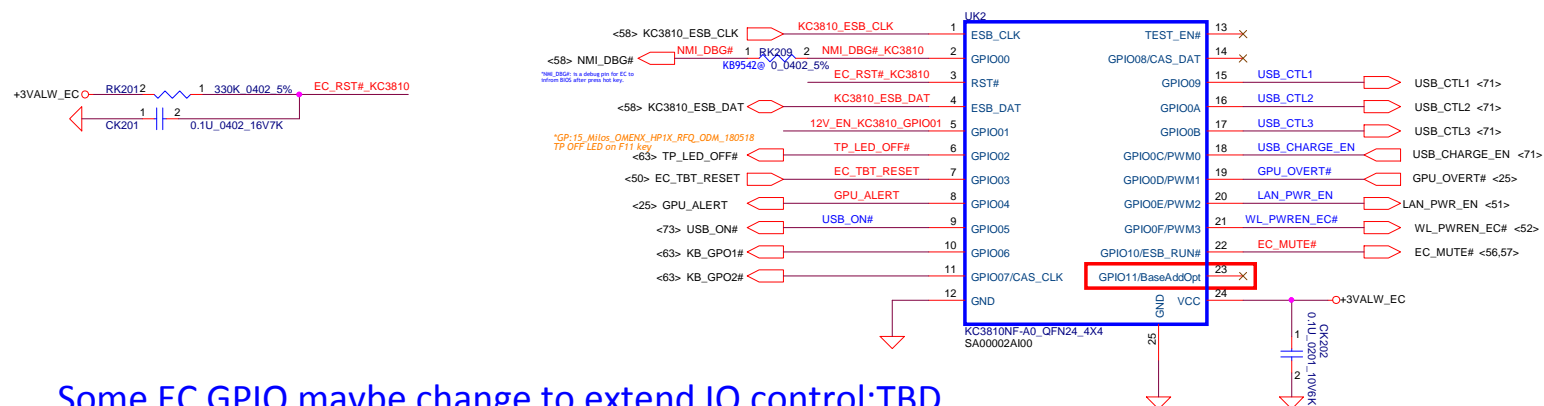
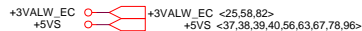
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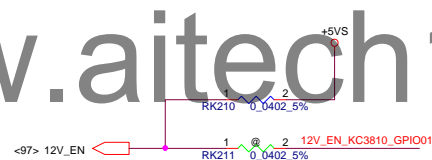






以下14個Pin 建議可以接到 external I/O 3810,

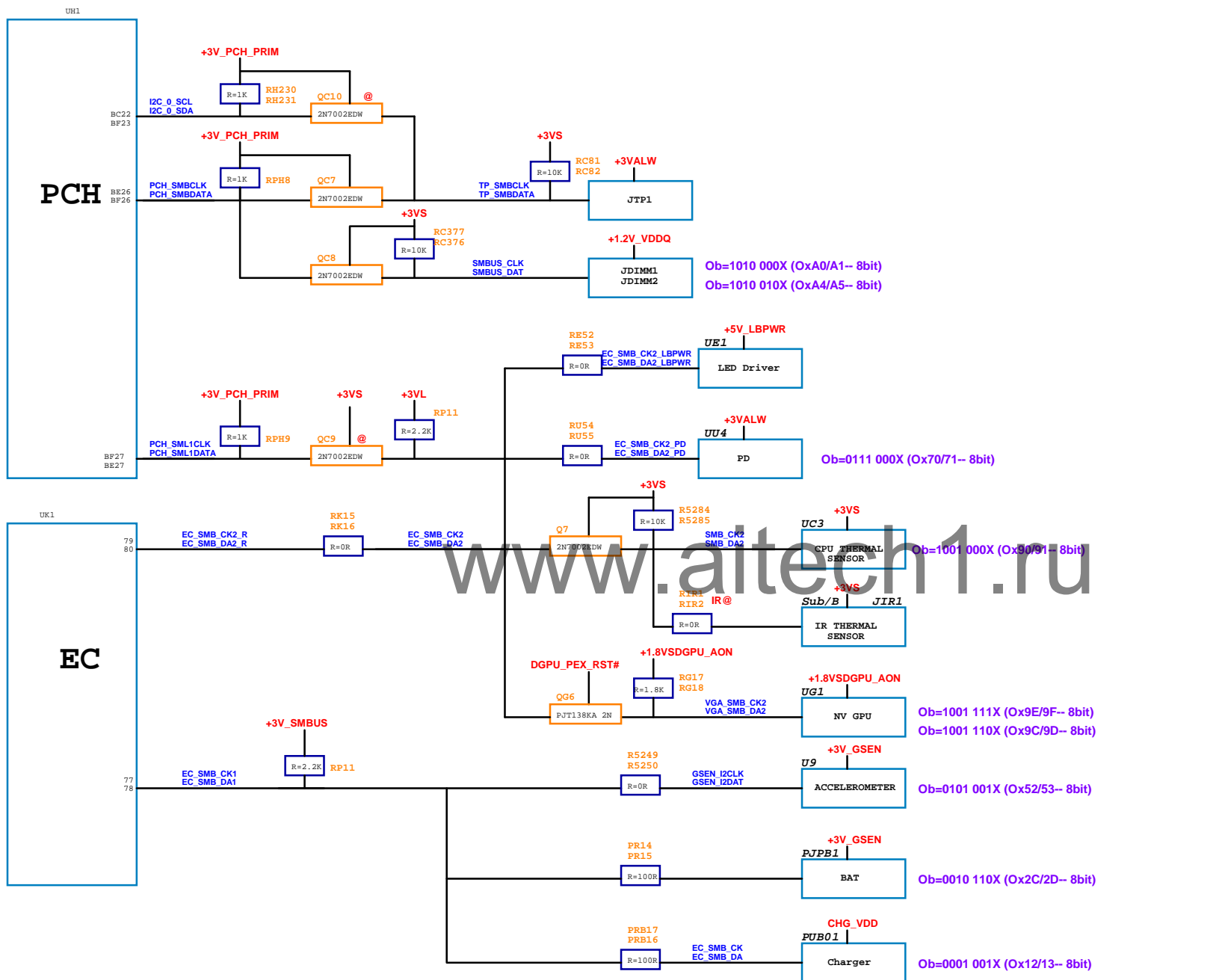
1. USB\_CTL1(GPIO4B Pin84),
2. USB\_CTL2(GPIO3F Pin72),
3. USB\_CTL3(GPIO1D Pin38),
4. USB\_CHARGE\_EN(GPIO1A Pin36),
5. GPU\_OVRN(GPIO0M Pin19) => DPFS0 NO USE
6. LAN\_PWR\_EN(GPIO4D Pin86),
7. WL\_PWREN\_EC(GPIO6I Pin98),
8. DCHG\_1(GPIO4O Pin73) => DPFS0 NO USE
9. USB\_ONH(GPIO37 Pin 121),
10. LED : 5 Pin.

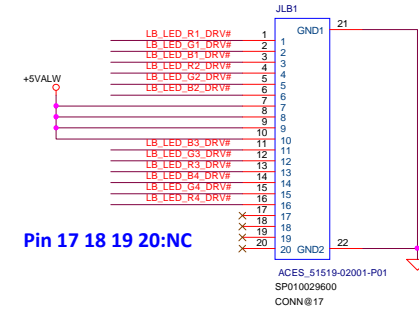
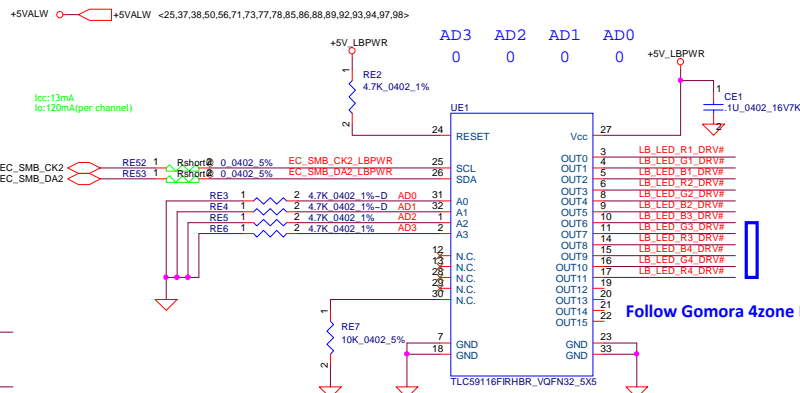
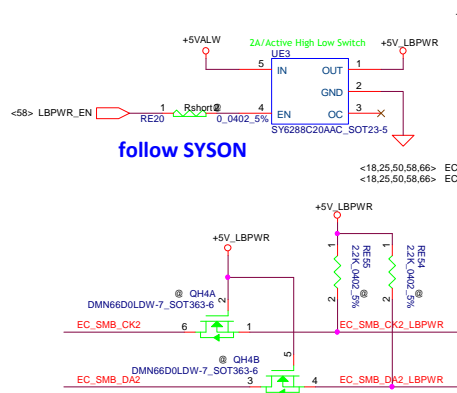


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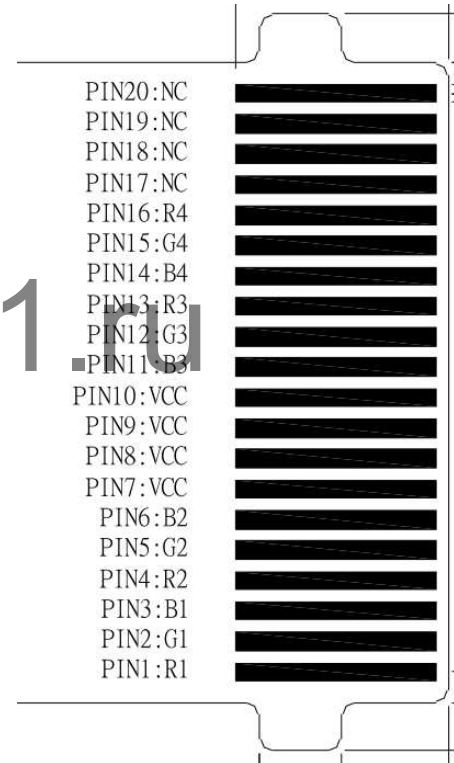
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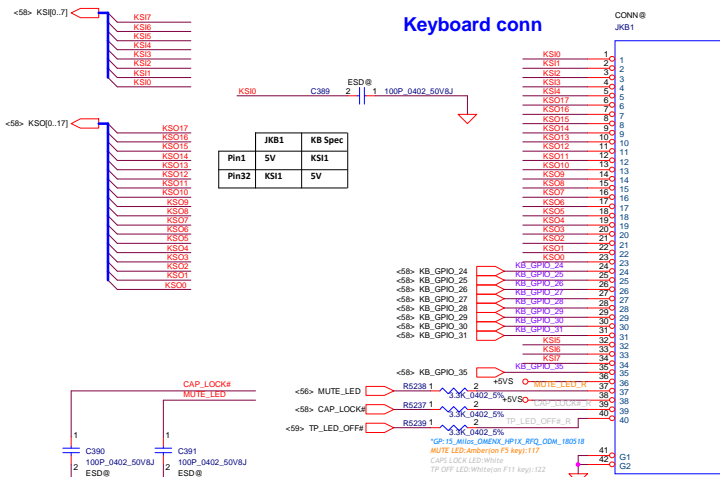


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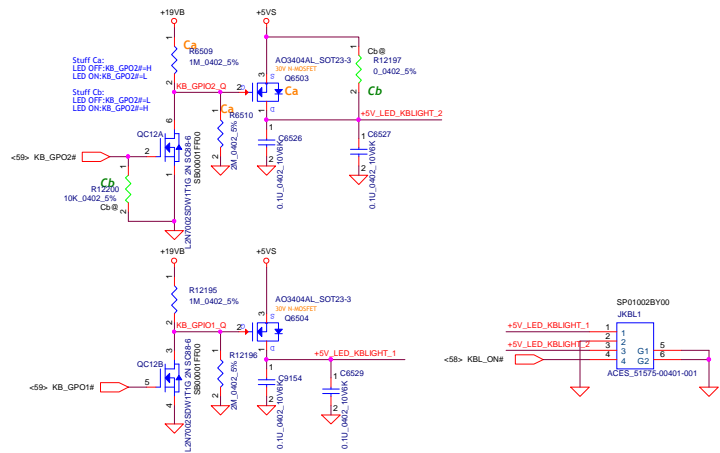




+3VALW		+3VALW <14,18,20,39,48,49,50,51,52,58,66,71,78,85,86,87,91,92,94,95>
+5VALW		+5VALW <25,37,38,50,56,62,71,73,77,78,85,86,88,89,92,93,94,97,98>
+5VS		+5VS <37,38,39,40,56,59,67,78,96>



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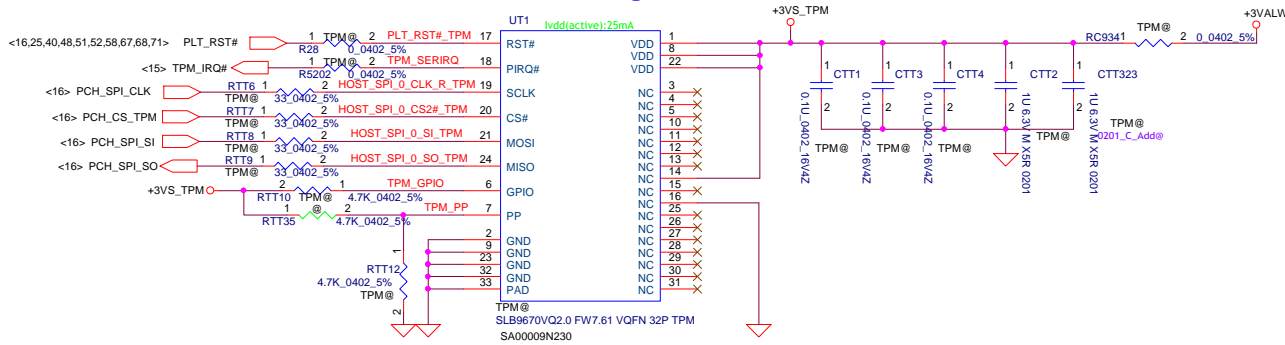
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# TPM2.0



# ACCELEROMETER ST Micro HP2DC

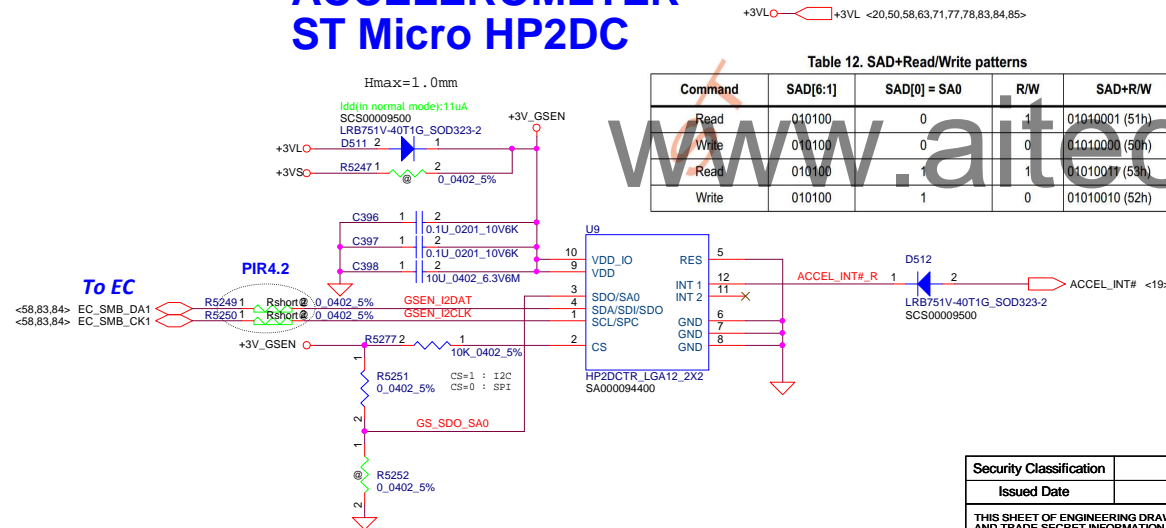
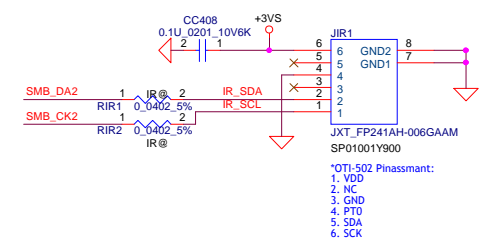
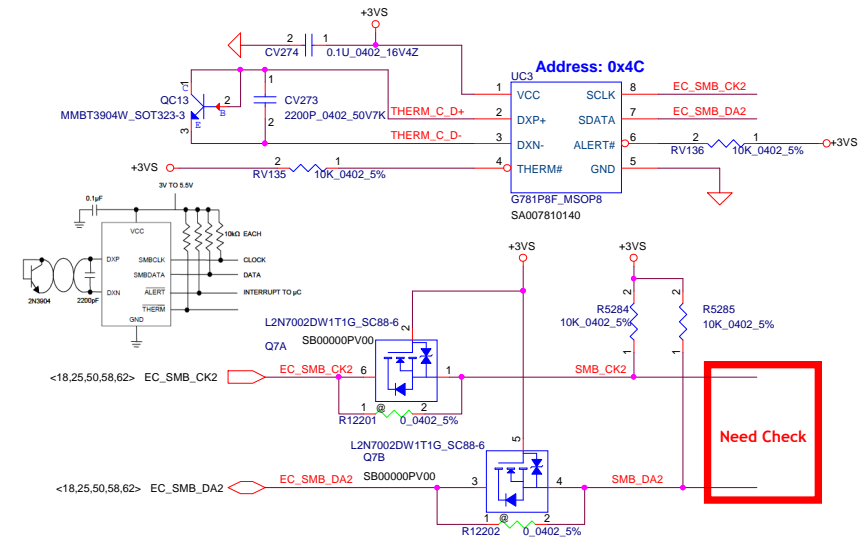


Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010001 (53h)
Write	010100	1	0	01010010 (52h)

# CPU THERMAL SENSOR



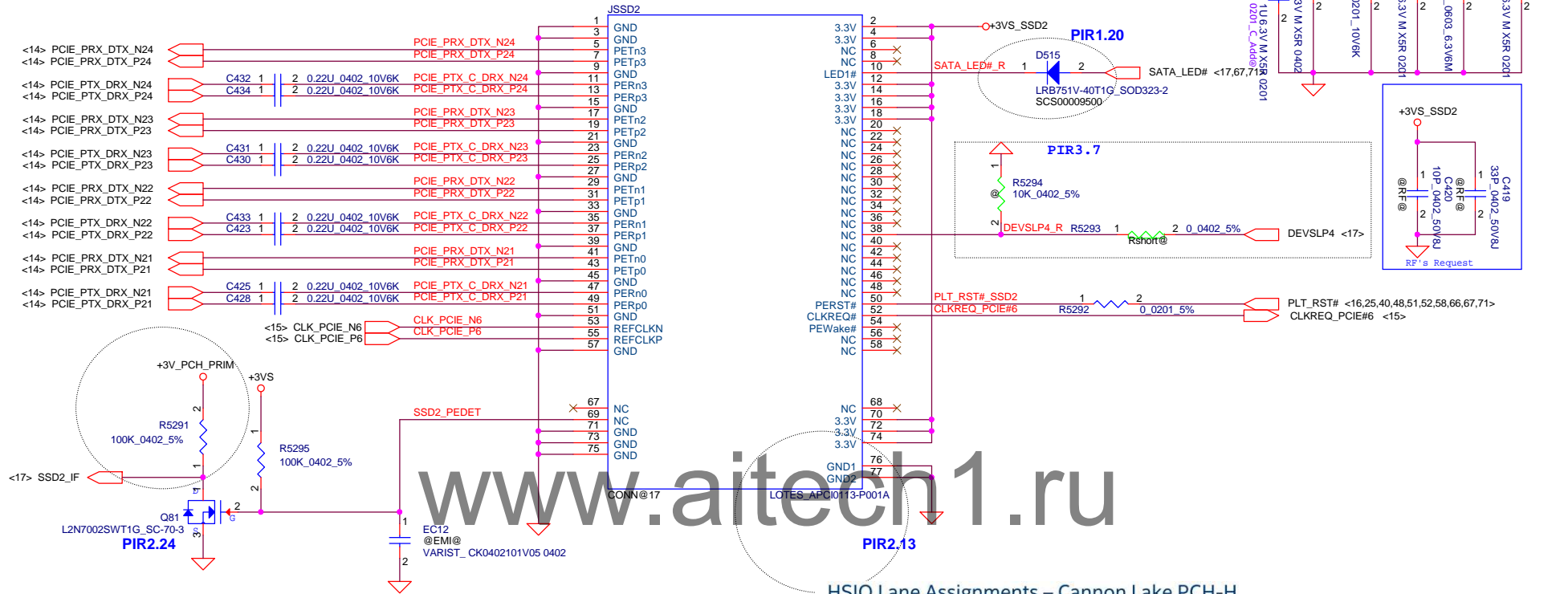
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# M.2 SSD:2

## Only support PCIe & Optane

+3V\_PCH\_PRIM <14,15,16,18,19,20,67,78,87>  
+3VS <10,15,16,17,18,19,22,23,24,25,37,38,40,42,48,49,51,56,57,58,66,67,71,77,78,88,92,94,95>



### 36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express\* Multiplexed Ports

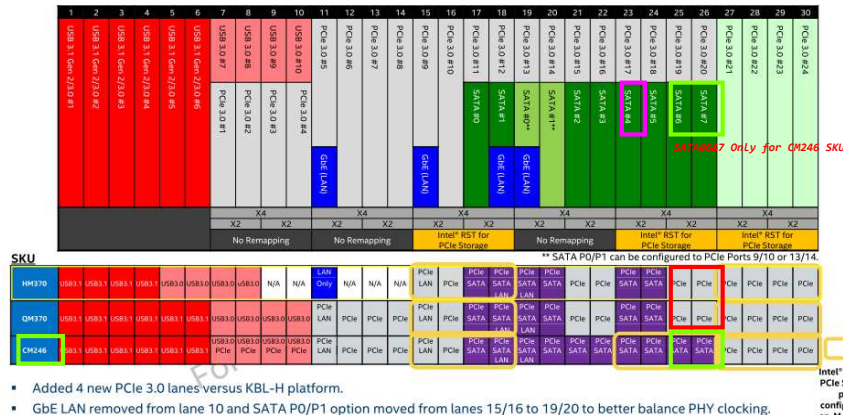
The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe\* multiplexed ports.

**Note:** When SATA and PCIe\* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

39	GND	Return Current Path	40	GND	Return Current Path
41	TXP	Transmitter Differential Signal Pair	42	TXN	Transmitter Differential Signal Pair
43	RXP	Receiver Differential Signal Pair	44	RXN	Receiver Differential Signal Pair
45	GND	Return Current Path	46	GND	Return Current Path
47	RXP	Receiver Differential Signal Pair	48	RXN	Receiver Differential Signal Pair
49	GND	Return Current Path	50	GND	Return Current Path
51	GND	Return Current Path	52	GND	Return Current Path

39	GND	Return Current Path	40	GND	Return Current Path
41	TXP	Transmitter Differential Signal Pair	42	TXN	Transmitter Differential Signal Pair
43	RXP	Receiver Differential Signal Pair	44	RXN	Receiver Differential Signal Pair
45	GND	Return current path	46	GND	Return current path
47	RXP	Receiver Differential Signal Pair	48	RXN	Receiver Differential Signal Pair
49	GND	Return current path	50	GND	Return current path
51	GND	Return current path	52	GND	Return current path

### HSIO Lane Assignments – Cannon Lake PCH-H



- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA P0/P1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

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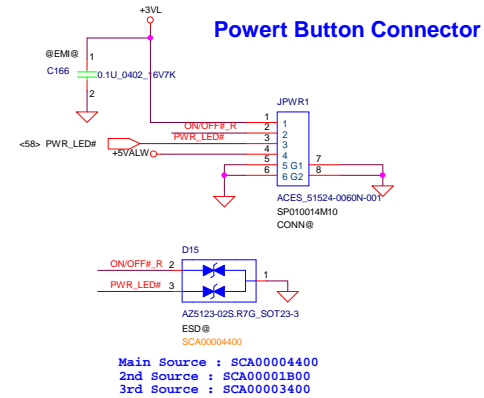
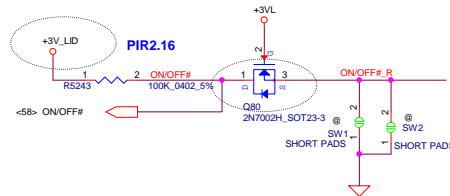


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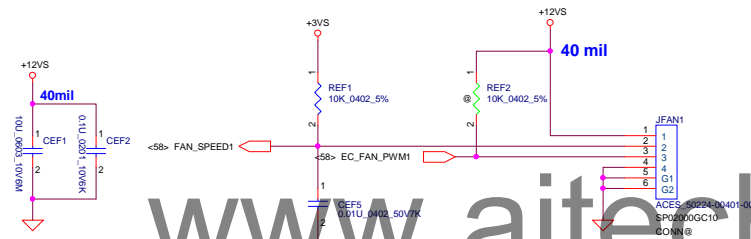
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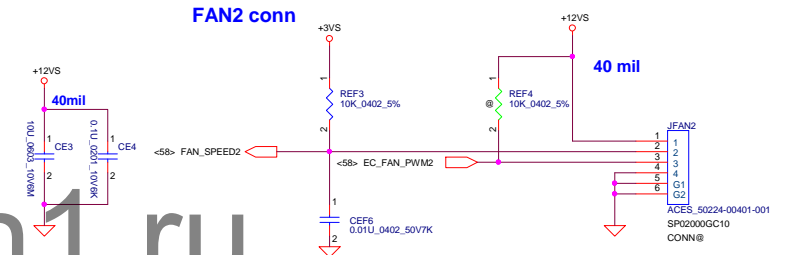
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**FAN1 conn**

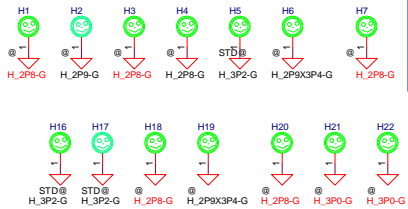


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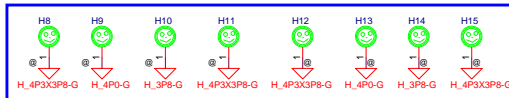


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## Screw Hole



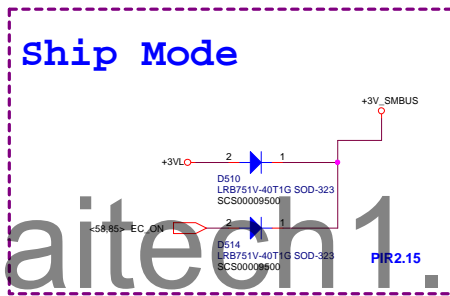
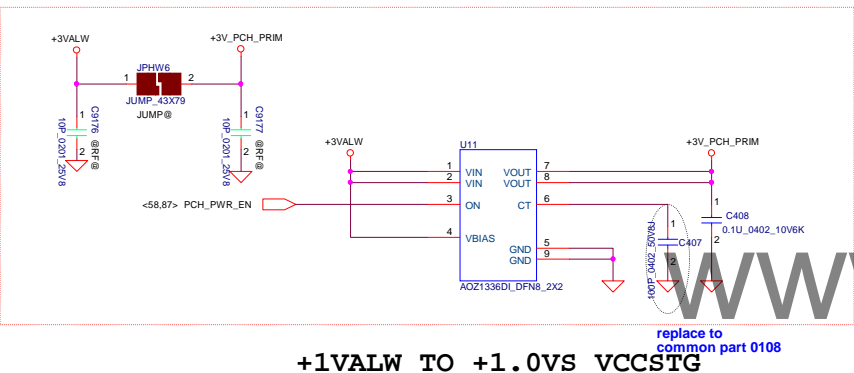
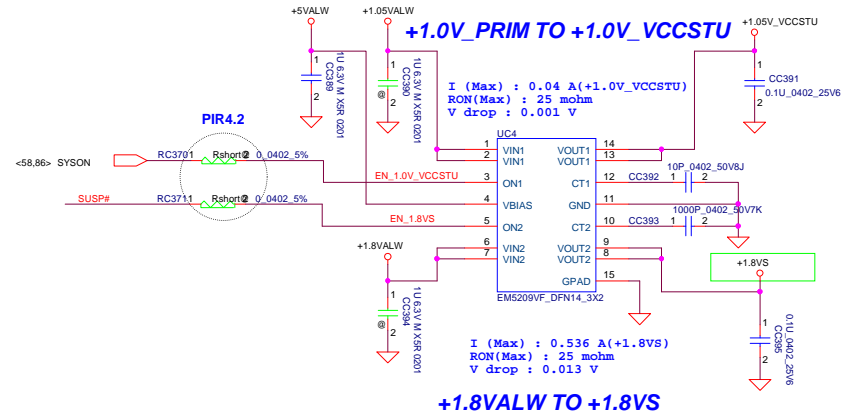
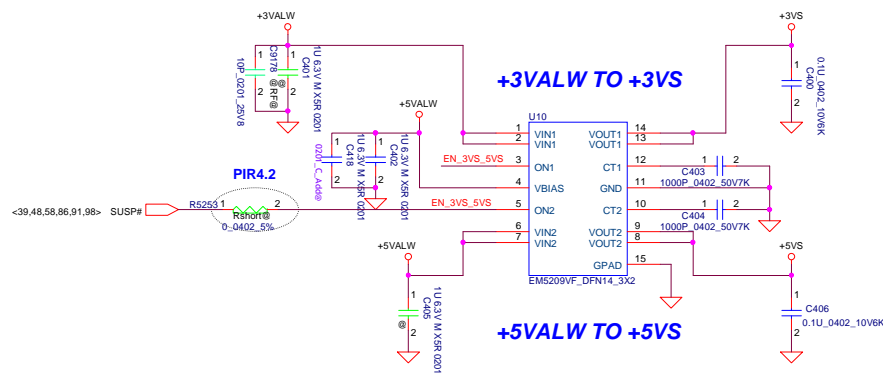
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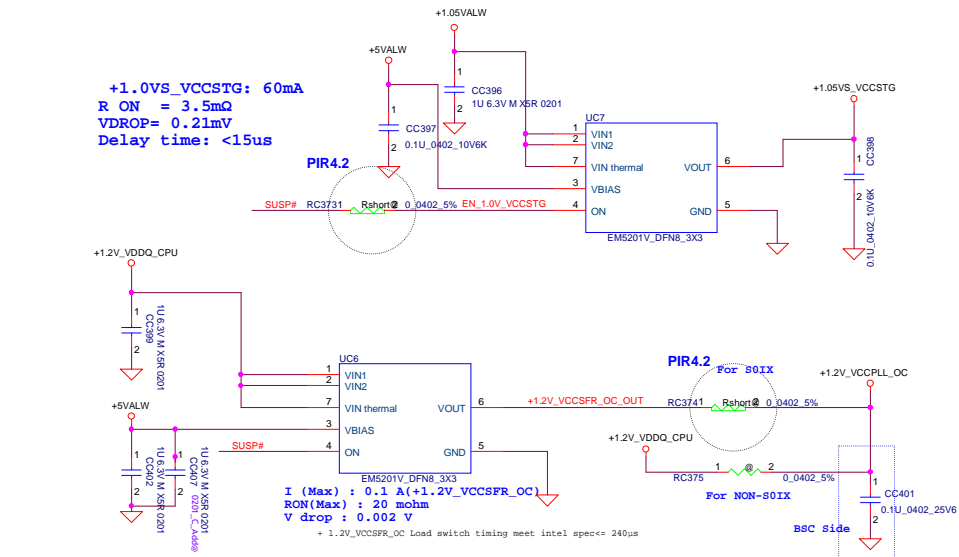
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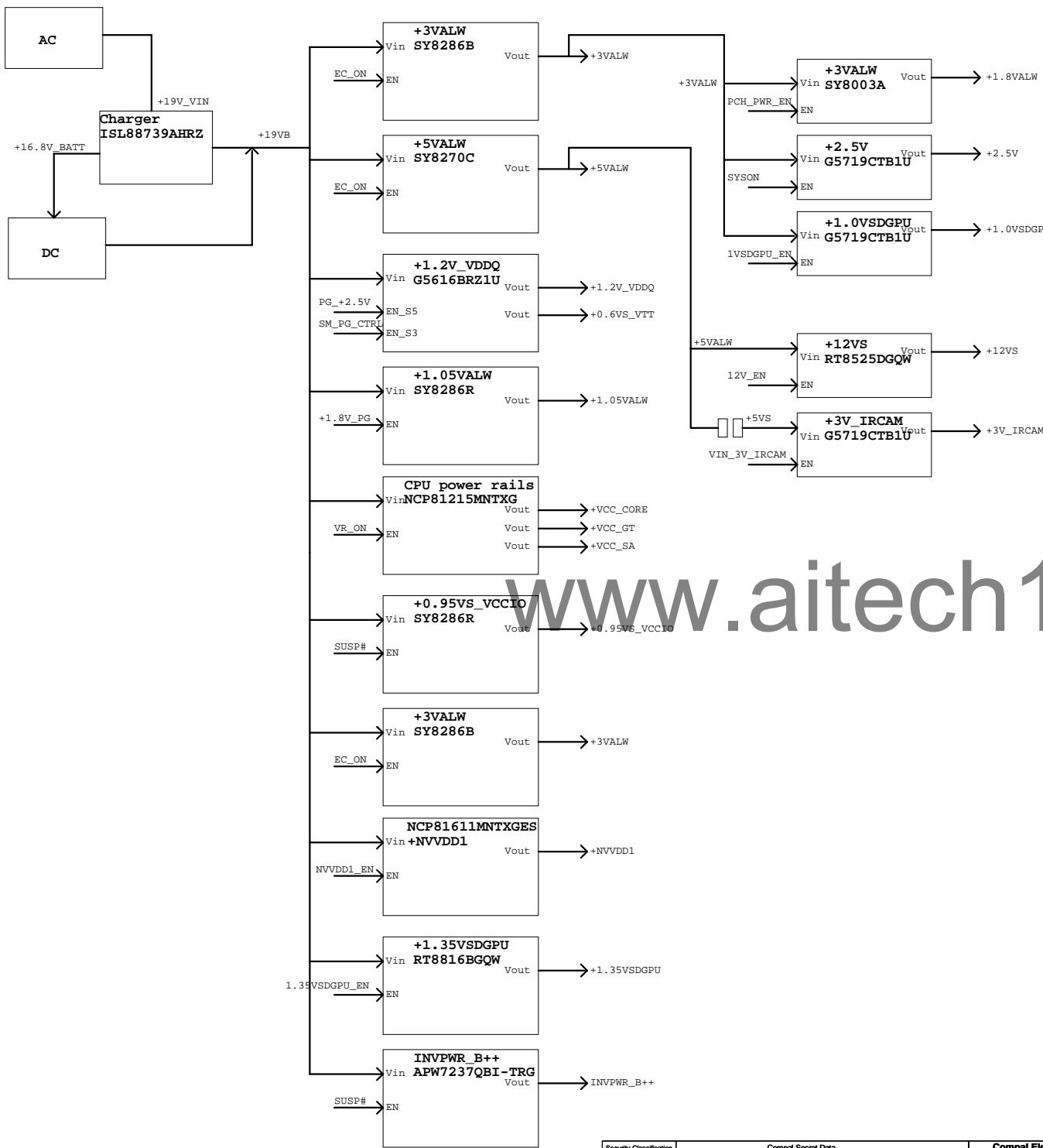
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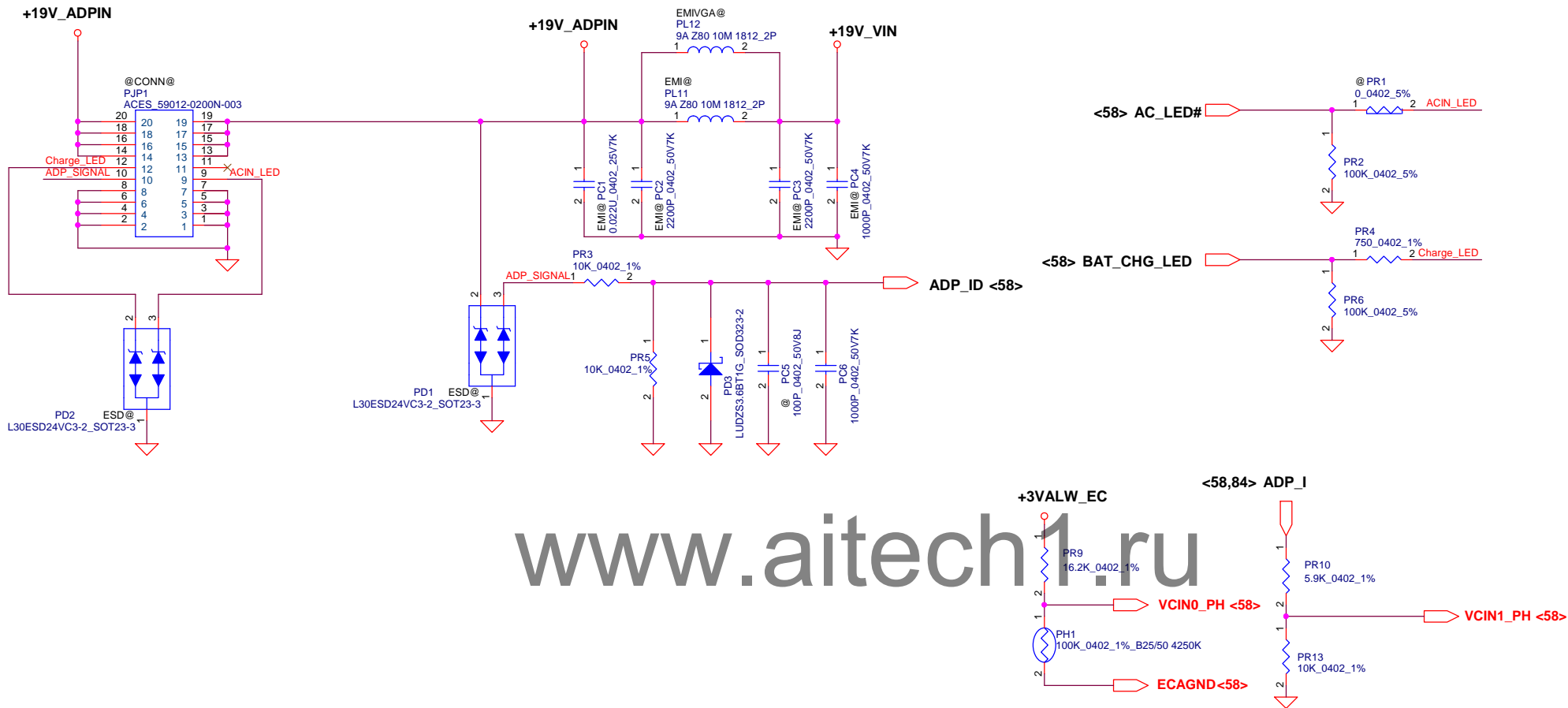
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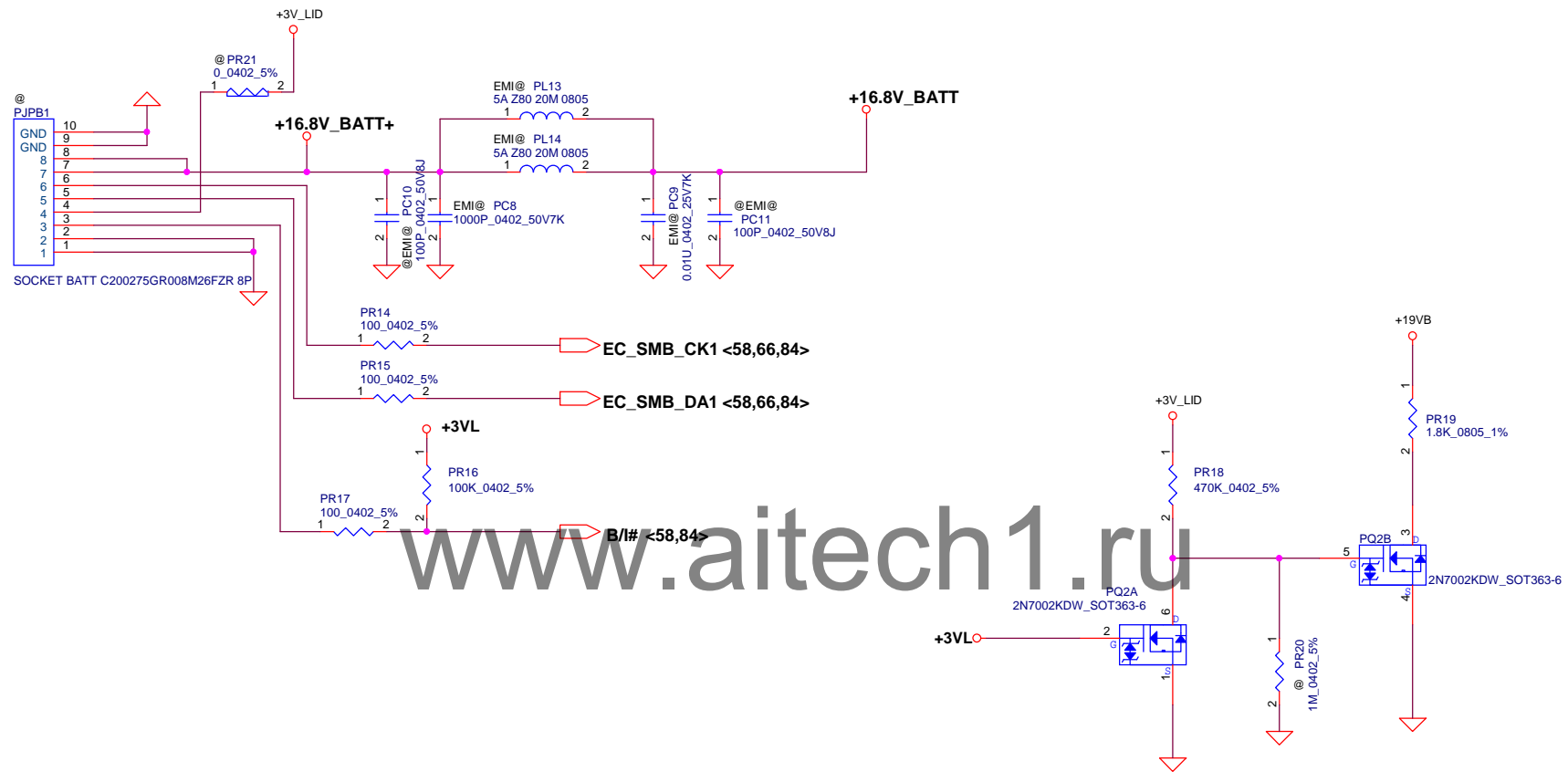


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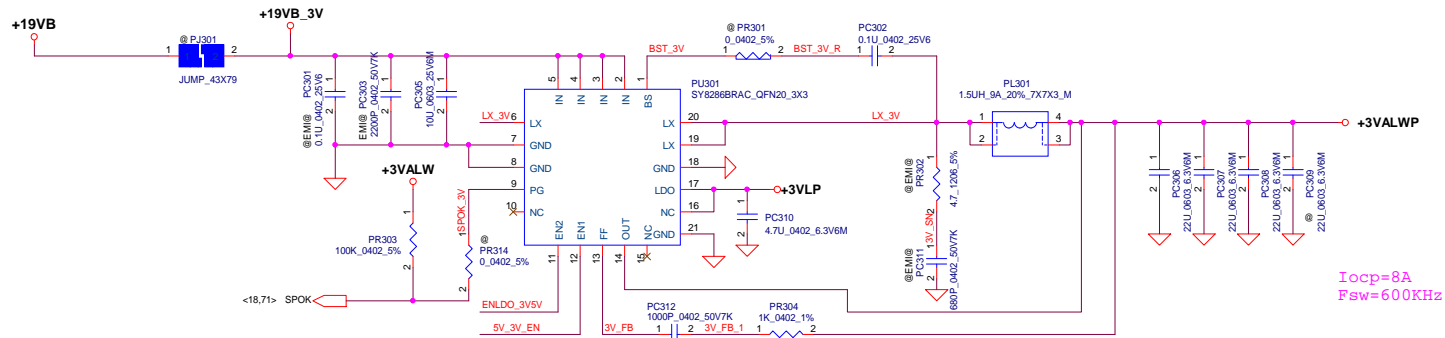


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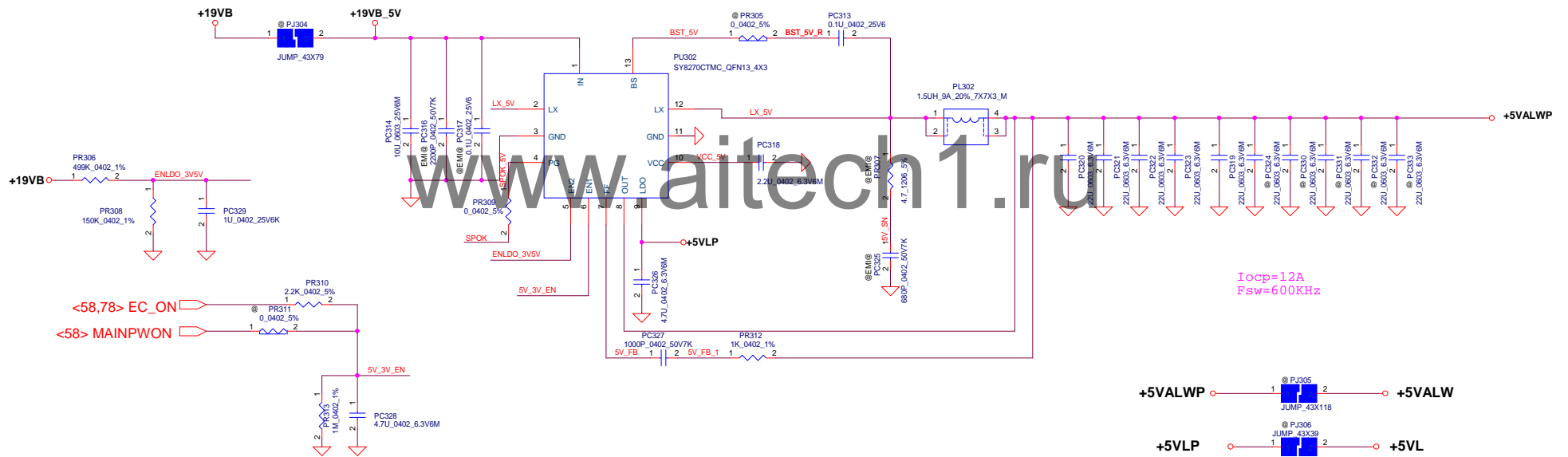
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**+3VALWP** **+3VALW**

**+3VLP** **+3VL**



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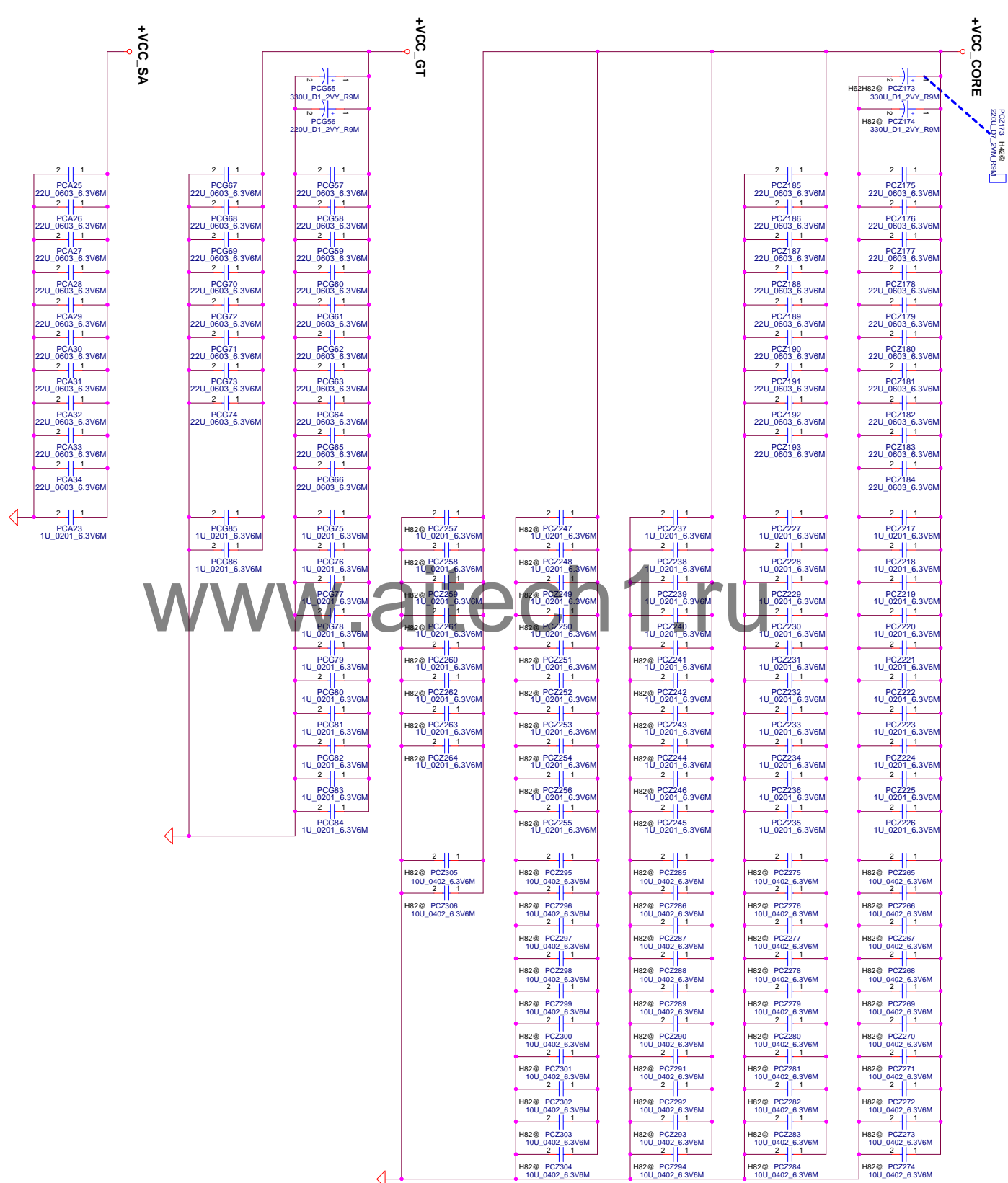




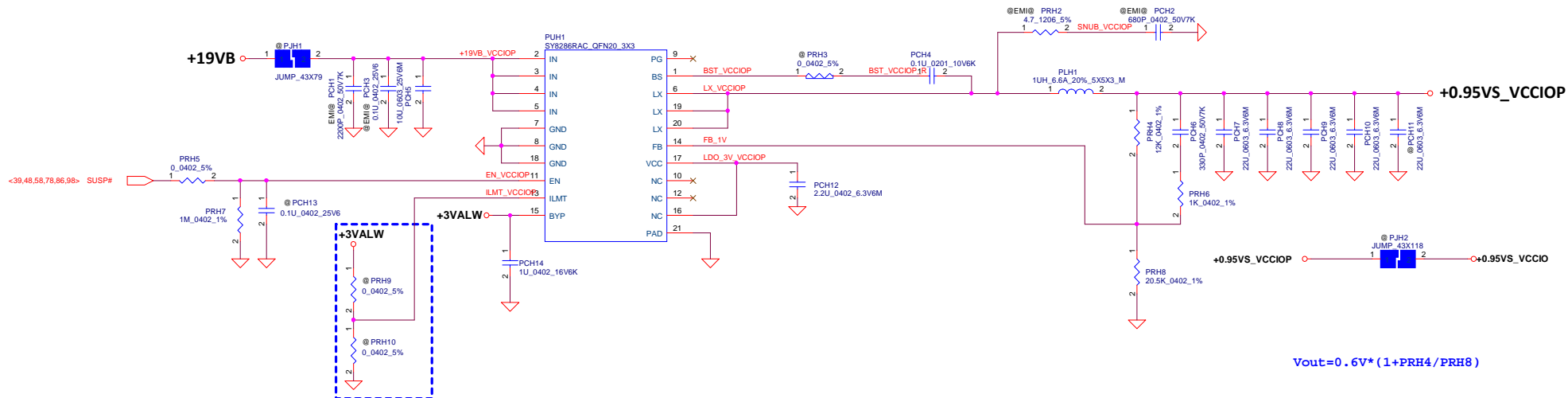
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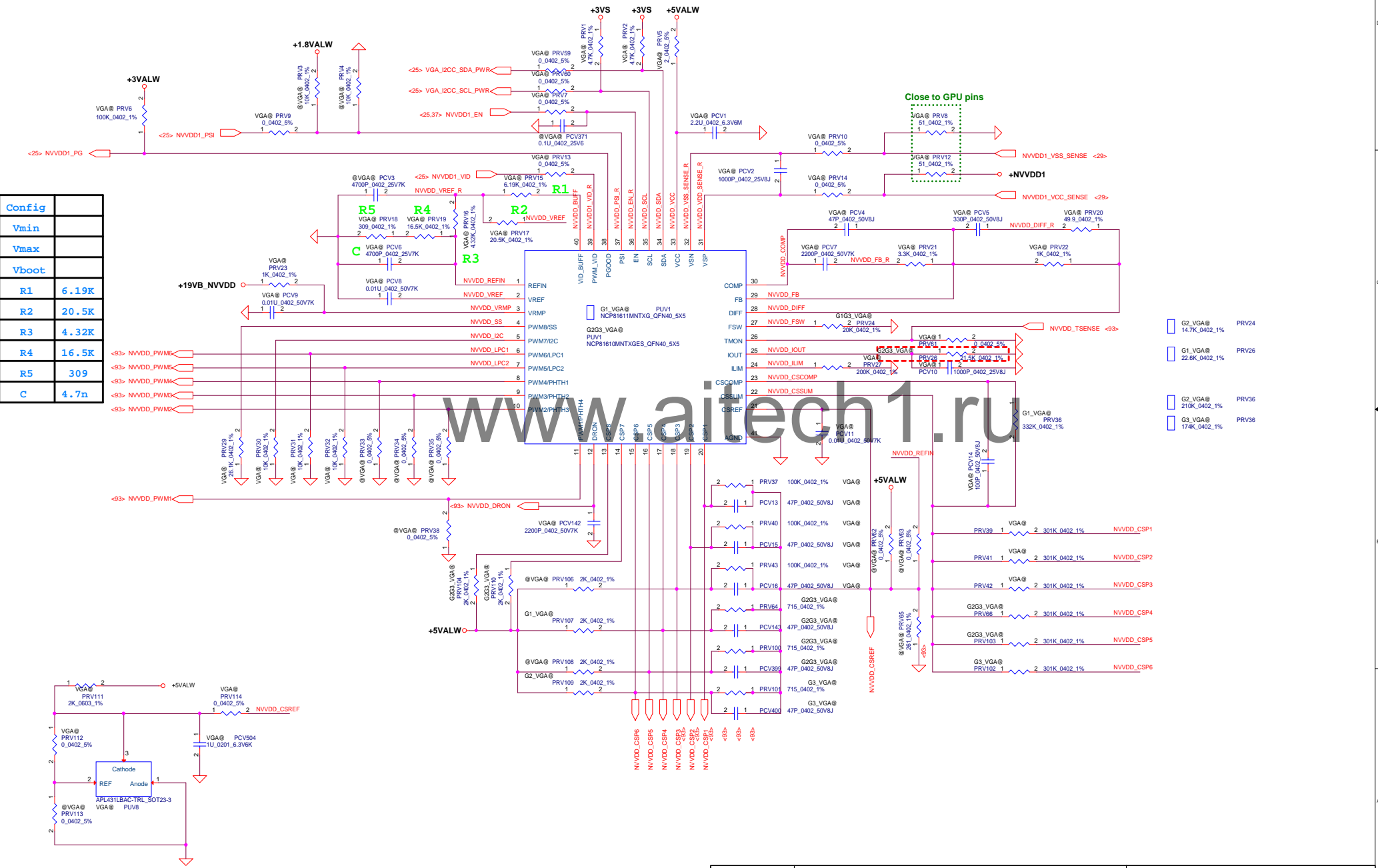
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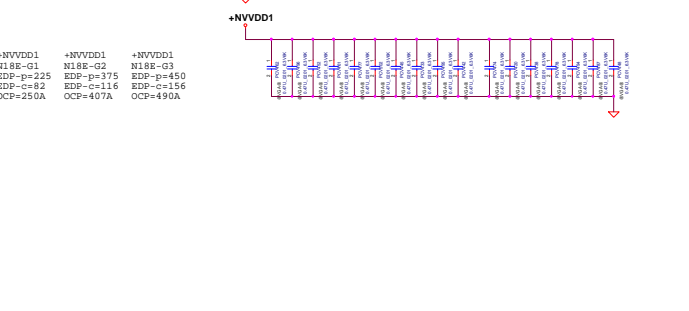
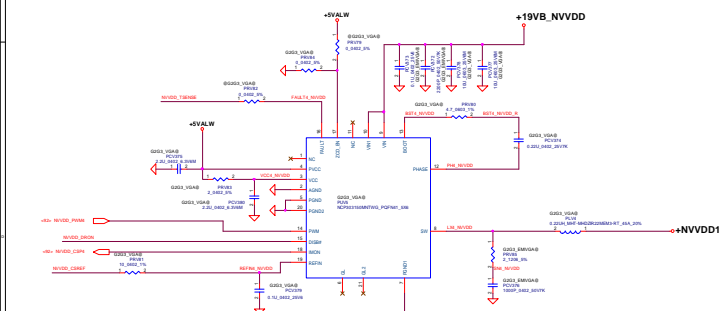
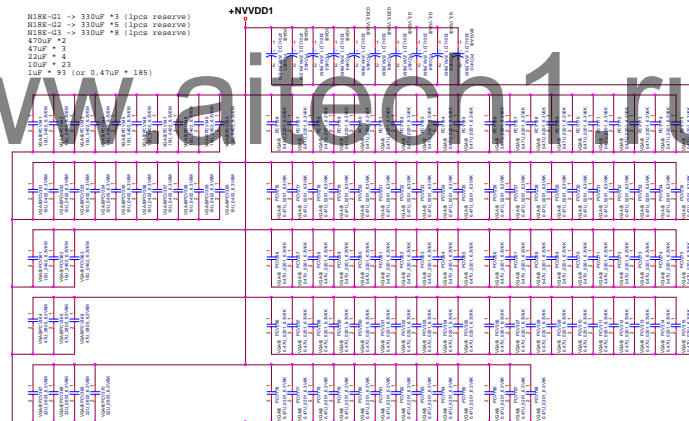
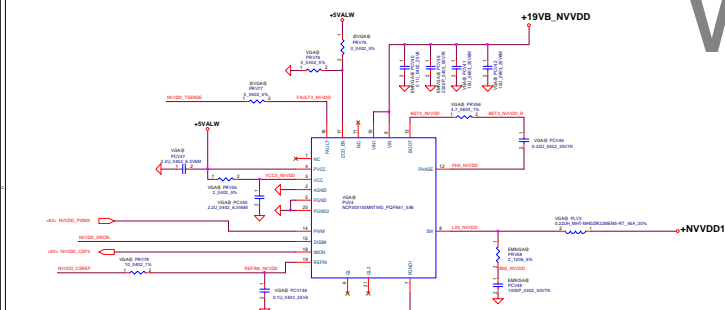
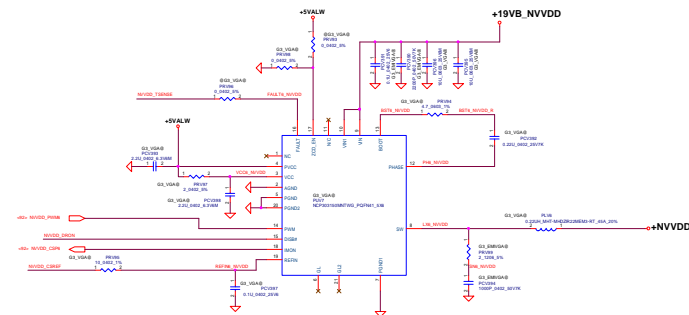
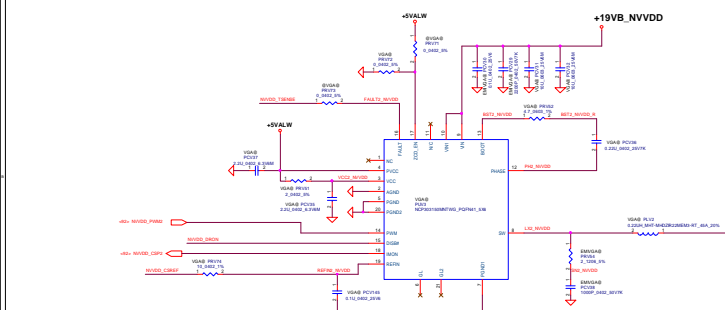
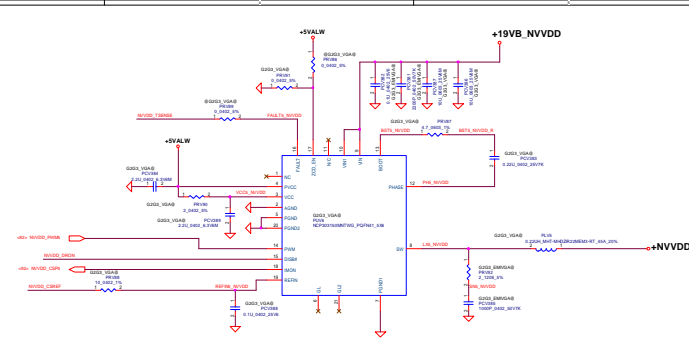
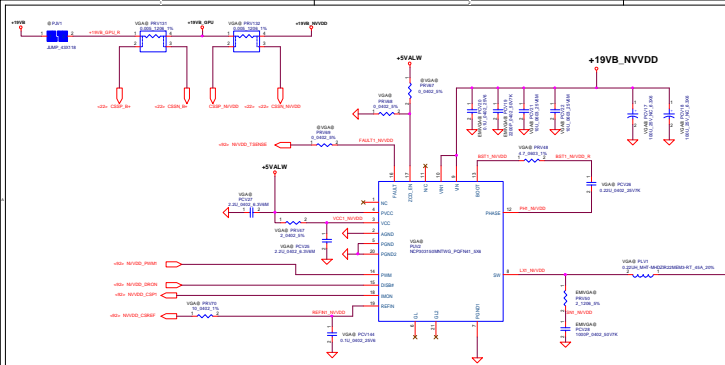


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Vmax	
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R4	16.5K
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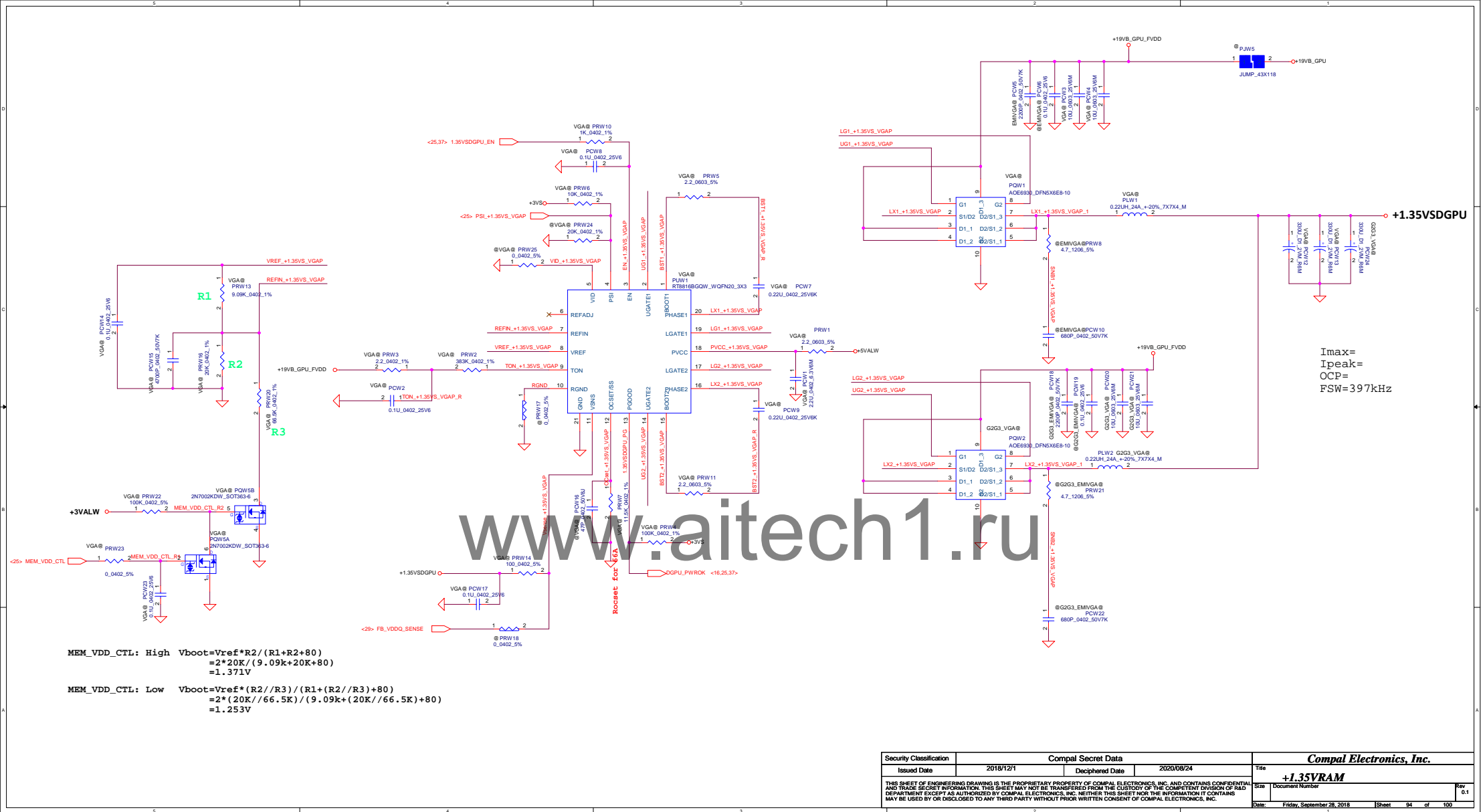


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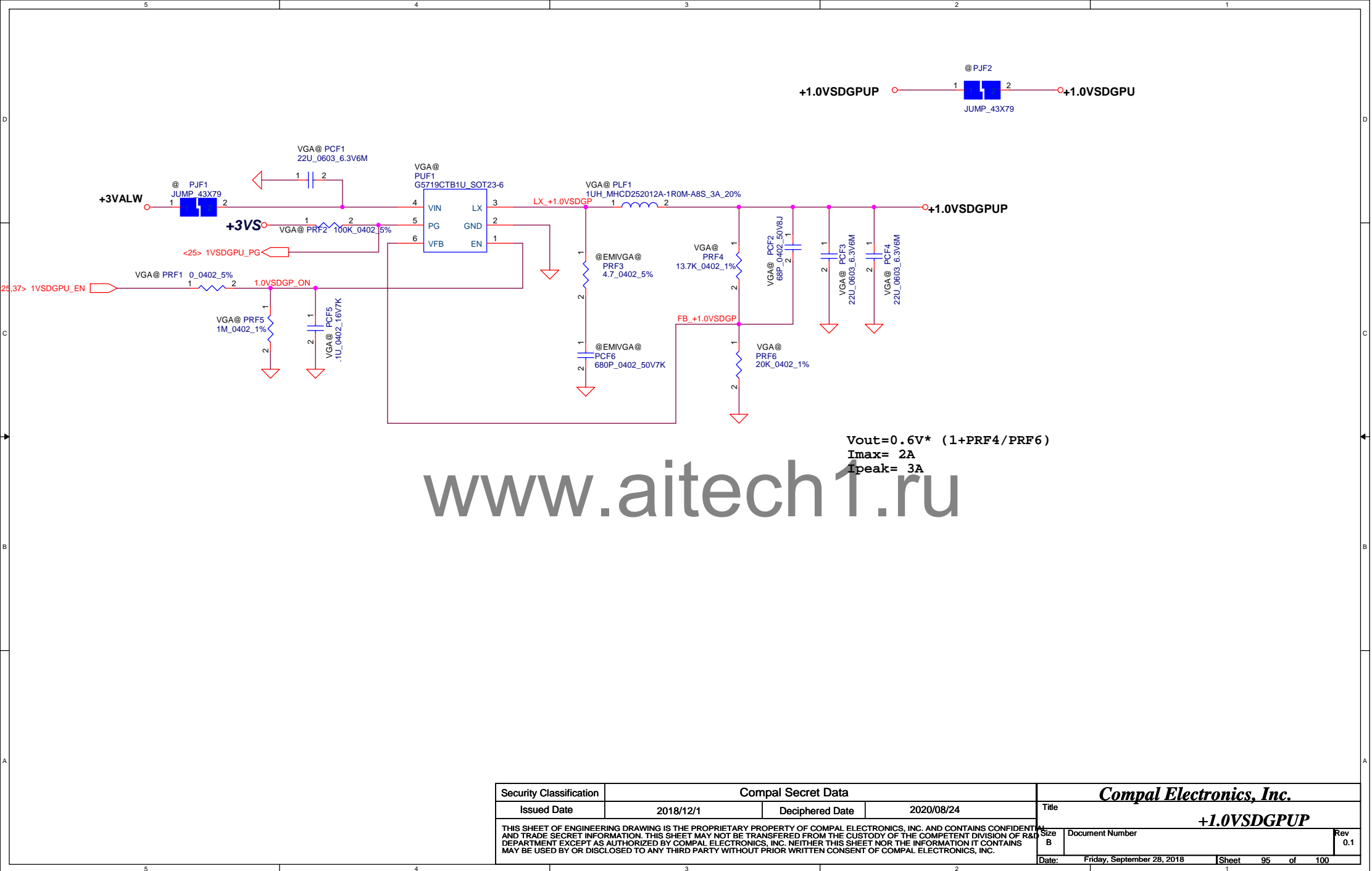
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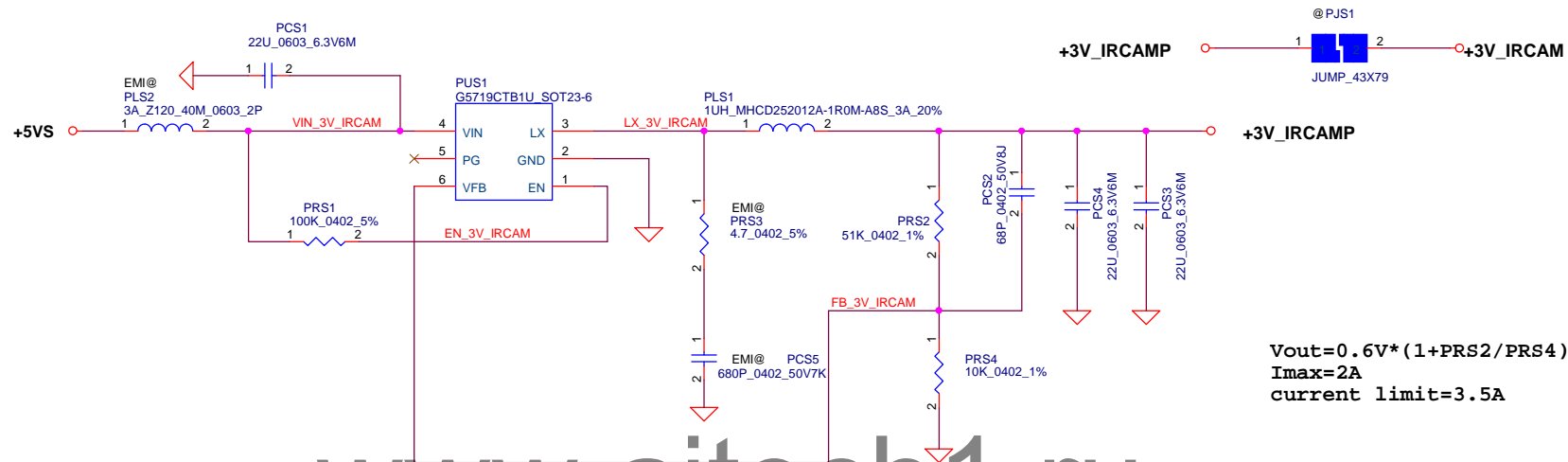
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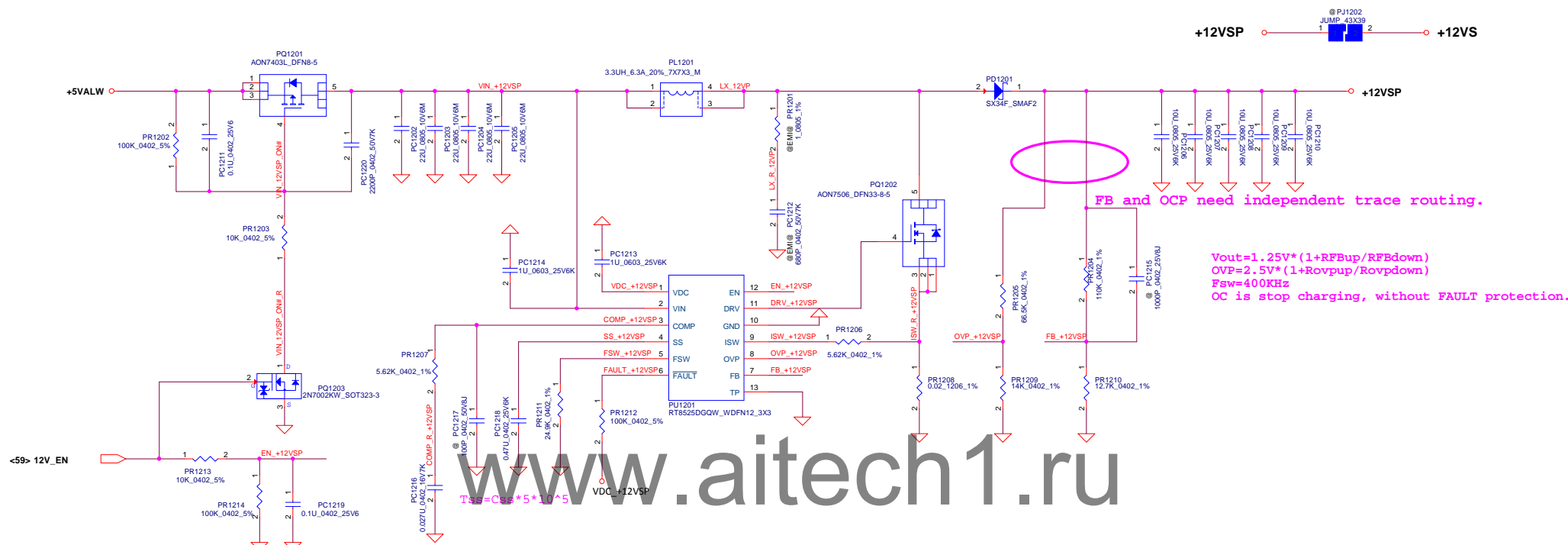


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